Developer Note

Power Macintosh 4400

1/29/97

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About This Note

This developer note describes the Power Macintosh 4400 computer, which is a new Macintosh model that uses a logic board based on the Apple Logic Board Design LPX-40.

This developer note describes the differences and similarities between features of the Power Macintosh 4400 computer and the Apple Logic Board Design LPX-40. The information in the Apple Logic Board Design LPX-40 developer note is repeated in chapters 2 through 4 of this developer note. If you are already familiar with the LPX-40 logic board, Chapter 1 provides you with the information required to understand the design features of the Power Macintosh 4400 computer.

This developer note is intended to help hardware and software developers design products that are compatible with the Macintosh products described here. If you are unfamiliar with Macintosh computers or would simply like more technical information, you may wish to read the related technical documents listed in the section “Supplemental Reference Documents.”

Contents of This Note

The information is arranged in four chapters and an index.

- Chapter 1, “Introduction,” gives a summary of the features of the Power Macintosh 4400 computer and discusses issues related to compatibility with other Macintosh computer software and hardware.
- Chapter 2, “Architecture,” describes the organization of the logic board. This chapter includes a block diagram and descriptions of the main components of the logic board.
- Chapter 3, “I/O Features,” describes the built-in input/output (I/O) device interfaces and the external I/O ports. It also describes the built-in video support for external video monitors.
- Chapter 4, “Expansion Features,” describes the expansion slots on the Power Macintosh 4400 computer logic board. This chapter provides descriptions of the supported DRAM, second-level cache, and I/O expansion slots and brief descriptions of the expansion modules for the other slots.

Supplemental Reference Documents

For a description of the version of the Mac OS that supports the Power Macintosh 4400 computer, developers should refer to Technote 1050.

Developers should have the relevant books of the *Inside Macintos*h series. You should also have *Designing PCI Cards and Drivers for Power Macintosh Computers*. These books are available in technical bookstores and through the *Apple Developer Catalog*. You should also have the *ATA Device Software Guide* if you plan to develop software utilities or drivers for ATA or ATAPI devices.

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dedicated to providing developers with up-to-date Apple documentation for existing and emerging Macintosh technologies. Developer World can be reached at

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Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in `Courier` font.

Hexadecimal numbers are preceded by a dollar sign ($). For example, the hexadecimal equivalent of decimal 16 is written as $10.

Note
A note like this contains information that is interesting but not essential for an understanding of the text. ◆

IMPORTANT
A note like this contains important information that you should read before proceeding. ▲

Standard Abbreviations

When unusual abbreviations appear in this book, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out. Here are the standard units of measure used in this developer note:

A	amperes	mA	milliamperes
dB	decibels	µA	microamperes
GB	gigabytes	MB	megabytes
Hz	hertz	MHz	megahertz
in.	inches	mm	millimeters
k	1000	ms	milliseconds
K	1024	µs	microseconds
KB	kilobytes	ns	nanoseconds
kg	kilograms	Ω	ohms

kHz	kilohertz	sec.	seconds
kΩ	kilohms	V	volts
lb.	pounds	W	watts

Here are other abbreviations that may used in this developer note:

$*n*	hexadecimal value *n*
AC	alternating current
ADB	Apple Desktop Bus
AV	audiovisual
AWACS	audio waveform amplifier and converter for sound
CD-ROM	compact disk read-only memory
CLUT	color lookup table
DAC	digital to analog converter
DAV	digital audio video
DDC	display data channel
DESC	digital video decoder and scaler
DIMM	dual inline memory module
DMA	dynamic memory access
DRAM	dynamic random-access memory
DVA	digital video application
EDO	extended data out DRAM device type
EMI	electromagnetic interference
FPU	floating-point unit
GCR	group code recording
GIMO	graphic internal monitor out (for PC compatibility cards)
IC	integrated circuit
IDE	integrated device electronics
IIC	inter-integrated circuit (an internal control bus)
I/O	input/output
IR	infrared
LS TTL	low-power Schottky TTL (a standard type of device)
MESH	Macintosh enhanced SCSI hardware
MFM	modified frequency modulation
MMU	memory management unit
MOS	metal-oxide semiconductor
NTSC	National Television Standards Committee (the standard system used for broadcast TV in North America and Japan)
NMI	nonmaskable interrupt

PAL	Phase Alternating Line system (the standard for broadcast TV in most of Europe, Africa, South America, and southern Asia)
PCI	Peripheral Component Interconnect
PDS	processor-direct slot
PLL	phase locked loop
PWM	pulse-width modulation
RAM	random-access memory
RGB	a video signal format with separate red, green, and blue components
RISC	reduced instruction set computing
RMS	root-mean-square
ROM	read-only memory
SANE	Standard Apple Numerics Environment
SCSI	Small Computer System Interface
SCC	serial communications controller
SECAM	the standard system used for broadcast TV in France and the former Soviet countries
SGRAM	synchronous graphics random access memory
SIMM	single inline memory module
S-video	a type of video connector that keeps luminance and chrominance separate; also called a Y/C connector
SWIM	Super Woz Integrated Machine, a custom IC that controls the floppy disk interface
TTL	transistor-transistor logic (a standard type of device)
VCR	video-cassette recorder
VLSI	very large scale integration
VRAM	video RAM; used for display buffers
Y/C	a type of video connector that keeps luminance and chrominance separate; also called an S-video connector
YUV	a video signal format with separate luminance and chrominance components

CHAPTER 1

Introduction

The Power Macintosh 4400 computer has a new logic board that incorporates a PowerPC™ 603e microprocessor, a second-level (L2) cache expansion slot, three DRAM expansion slots, one PCI communications slot, two Peripheral Component Interconnect (PCI) card expansion slots, standard Macintosh I/O ports, and support for an internal ATAPI CD-ROM drive. The Power Macintosh 4400 logic board layout follows the LPX form factor.

Summary of Features

Here is a summary of the hardware features of the Power Macintosh 4400 computer. Each feature is described more fully later in this note.

- Microprocessor: PowerPC 603e microprocessor running at 200 MHz.
- RAM: 0 MB soldered to the main logic board; expandable to 160 MB using 168-pin JEDEC-standard 3.3 volt unbuffered EDO (extended data out) DIMM (dual inline memory module) devices. Three DIMM slots are provided for DRAM expansion.
- ROM: 4 MB soldered on main logic board; 64-bit ROM data bus width.
- Cache: 256 KB L2 cache on a 160-pin DIMM card (optional).
- Macintosh standard 15-pin monitor connector.
- Video display modes: the Power Macintosh 4400 computer provides support for a wide range of displays depending on the amount of video RAM installed. For a complete description of the display modes and pixel resolutions supported by the Power Macintosh 4400 computer, see “Video Display Resolution” on page 38.
- 2D built-in graphics acceleration.
- Sound: 16 bits/channel stereo sound input and output, external rear jack for sound in, rear jack for headphones or amplified stereophonic speakers, and one built-in speaker.
- Hard disks: one internal 3.5-inch IDE hard disk with 1.2 GB or larger capacity; external SCSI port (DB-25) for additional SCSI devices. PIO, singleword DMA, and multiword DMA data transfers are supported.
- CD-ROM drive support: internal 8X-speed ATAPI CD-ROM drive.
- PCI card expansion slots: accepts two 7-inch PCI cards, or one 7-inch and one 12-inch PCI card.
- PCI communications slot for comm slot II cards.
- Floppy disk support: one internal 1.4 MB Apple SuperDrive.
- Processor bus: 64-bit wide, 40 MHz, supporting split address and data tenures.
- Standard Macintosh I/O ports: two GeoPort serial ports, sound input and output jacks, a SCSI port, and an ADB port.
- Apple GeoPort: supported on the Macintosh printer and modem serial ports.
- Power switch: support for soft power from keyboard and power switch.

- Voltage switch: allows selection of either 115 for voltages of 100-130 V or 230 for voltages of 200-230 V depending on the voltage that you will be connecting to. The voltage selection must be set manually on the power supply.
- Energy saving: sleep, startup, and shutdown scheduling can be controlled with an Energy Saver control panel.

Comparison With Apple Logic Board Design LPX-40

The main logic board in the Power Macintosh 4400 computer is based on the Apple Logic Board Design LPX-40. Table 1-1 compares the features of the Power Macintosh 4400 computer with the features of Apple Logic Board Design LPX-40.

Table 1-1 Comparison with the Apple Logic Board Design LPX-40

Features	Apple Logic Board Design LPX-40	Power Macintosh 4400 computer
Processor type	PowerPC 603e or 604e	PowerPC 603e
Processor speed	160 MHz, 180 MHz, and 200 MHz	200 MHz
Cache	256 KB L2 cache (optional)	256 KB L2 cache (optional)
Amount of RAM	0 MB–96 MB	0 MB–160 MB
RAM expansion	3 168-pin 3.3 volt unbuffered EDO DIMMs	3 168-pin 3.3 volt unbuffered EDO DIMMs
Memory bus	64 bits, 40 MHz	64 bits, 40 MHz
Video RAM	1 MB expandable to 4 MB (EDO DRAM, SDRAM, or SGRAM depending on logic board configuration)	1 MB expandable to 4 MB (EDO DRAM, SDRAM, or SGRAM depending on logic board configuration)
Video input	None (third-party PCI cards)	None (third-party PCI cards)
Video output	Depending on the amount of video RAM installed, the built-in video supports up to 1280-by-1024 pixel resolution at 16 bits per pixel	Depending on the amount of video RAM installed, the built-in video supports up to 1280-by-1024 pixel resolution at 16 bits per pixel
Graphics acceleration	2D graphics acceleration	2D graphics acceleration
Sound capabilities	8 or 16 bits / channel; stereo in, stereo record, stereo out	8 or 16 bits / channel; stereo in, stereo record, stereo out
Remote control	None	None

continued

Table 1-1 Comparison with the Apple Logic Board Design LPX-40 (continued)

Features	Apple Logic Board Design LPX-40	Power Macintosh 4400 computer
Floppy disk drive	1, internal (MFM or GCR)	1, internal (GCR)
ADB ports	1	1
PS/2 ports	2, for PS/2 keyboard and mouse	None
Internal hard disk	Supports 1 (IDE/ATA)	Supports 1 (IDE/ATA)
Internal CD-ROM	Supports 1 (ATAPI)	Supports 1 (ATAPI)
Internal SCSI expansion bay	None	None
External SCSI ports	1	1
Expansion slots	3 or 5 PCI slots for 7-inch or 12-inch PCI cards, depending on the riser card in the enclosure	2 PCI slots for 7-inch or 12-inch PCI cards, 1 PCI communications slot for PCI comm slot II cards
DMA I/O	10 DMA channels	10 DMA channels
Serial ports	2, LocalTalk and GeoPort supported	2, LocalTalk and GeoPort supported

Compatibility Issues

This section describes key issues you should be aware of to ensure that your hardware and software work properly with the logic board in the Power Macintosh 4400 computer. Some of the topics described here are covered in more detail in later parts of this developer note.

The gestalt value for the Power Macintosh 4400 computer is 515.

Communications Slot

The communications slot in the Power Macintosh 4400 computer is a PCI bus compatible communications slot (comm slot II) and is in general not compatible with communication cards for the Macintosh LC family of computers, the Macintosh Quadra 630 computer, or cards that operate in the communications slot (comm slot I) in Power Macintosh 5200 and 6200 computers. The exception is that cards that do not use the bus, such as serial modem cards, can be designed to work in both comm slot I and comm slot II. For more information about designing serial modem cards that are compatible with both communications slots, see the *Power Macintosh 5500 and 6500 Developer Note*. The comm slot on the PCI riser card in the Power Macintosh 4400

computer is electrically the same as the comm slot in the Power Macintosh 5400, 5500, and 6500 and the Macintosh Performa 6400 computers.

DRAM Expansion

The Power Macintosh 4400 computer requires 168-pin 3.3 volt unbuffered EDO (extended data out) JEDEC-standard DRAM DIMM cards, like those required for the Apple Logic Board Design LPX-40, rather than the 168-pin 5 volt fast-page DIMM cards used in the Power Macintosh 5400, 7600, 8500, and 9500 computers and the Macintosh Performa 6400. The connector notches have different offsets to differentiate between device types and to ensure that the correct devices are installed on the logic board. For information about DRAM DIMM configurations supported in the Power Macintosh 4400 computer, see “DRAM DIMMs” on page 40.

The Power Macintosh 4400 computer has three DRAM expansion slots. DRAM expansion slot 1 supports single-bank DIMMs (a maximum of 32 MB). DRAM expansion slots 2 and 3 support both single-bank and dual-bank DIMMs (a maximum of 64 MB per slot with dual-bank DIMMs). A total of 160 MB of DRAM is supported. No DRAM is soldered on the main logic board.

DRAM DIMM developers should note that the PSX memory controller on the logic board does not provide support for 4 M by 4 bits with 12-by-10 addressing, 1 M by 16 bits with 12-by-8 addressing, or with 11-by-9 addressing DRAM devices.

The limit of 16 address-line loads per DIMM slot for the Apple LPX-40 Logic Board Design has been increased on the Power Macintosh 4400 logic board to support 32 address-line loads per DIMM slot. This allows 64 MB DIMMs, consisting of thirty-two 4 M by 4 bit DRAM devices, to be used in the dual-bank DIMM slots on the Power Macintosh 4400 logic board.

DRAM DIMM Dimensions

The JEDEC MO-161 specification shows three possible heights for the 8-byte DIMM. For Macintosh computers, it is recommended that developers use only the shortest of the three: 1.100 inches. Taller DIMMs could put excessive pressure on the DIMM sockets due to possible mechanical interference inside the case.

Cache Expansion

The Power Macintosh 4400 computer supports an optional 256K second-level DIMM cache card that includes an integrated cache controller. Apple does not support development of third-party cache cards for the Power Macintosh 4400 computer. The 160-pin cache expansion slot is the same as the cache slot found in the Power Macintosh 5400 and Macintosh Performa 6400 computer models.

ATA (IDE) Hard Disk and ATAPI CD-ROM Drive

The interface for the internal hard disk and CD-ROM drive on the Power Macintosh 4400 computer logic board is ATA (IDE) for the hard disk and ATAPI for the CD-ROM, not SCSI. This could cause compatibility problems for disk utility programs. The system software release for computers equipped with the Power Macintosh 4400 computer includes version 3.1 or greater of the ATA Manager and supports PIO, singleword DMA, and multiword DMA data transfers. For more information about the software that controls ATA devices, see the *ATA Device Software Guide,* which can be found on the Apple Developer World Wide web site.

Video Display RAM

In addition to 2D graphics acceleration, the Power Macintosh 4400 computer uses the same video RAM DIMM expansion implementation that is used on the Apple Logic Board Design LPX-40. It supports expansion of up to 4 MB of video RAM through a variety of video RAM devices. The Power Macintosh 4400 computer also supports DDC (display data channel) plug-and-play monitor identification.

For additional information about video display resolution and video display sense codes supported by the Power Macintosh 4400 computer, see “Built-in Video” beginning on page 34. For a description of the video RAM DIMM connector, see “Video RAM” on page 50.

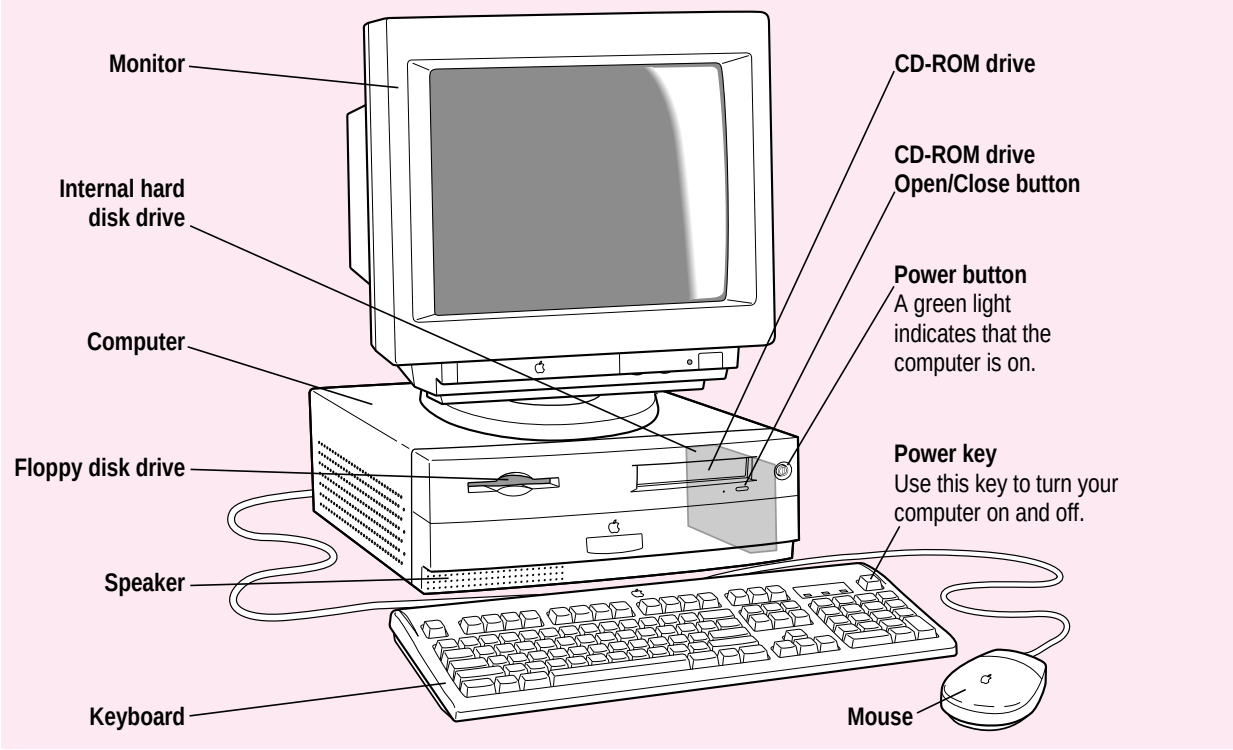
External Features

The Power Macintosh 4400 computer has a new compact design enclosure simular in size to other Power Macintosh desktop computers. The front bezel is plastic and the case is painted metal. The chassis includes heavy internal bracing, which easily supports 17 and 20-inch monitors.

Front View

Figure 1-1 is a front view of a Power Macintosh 4400 computer. The front view shows the location of the openings for the CD-ROM drive and floppy disk, the CD-ROM open and close button, and the power button with incorporated power-on light.

Figure 1-1 Front view of the computer

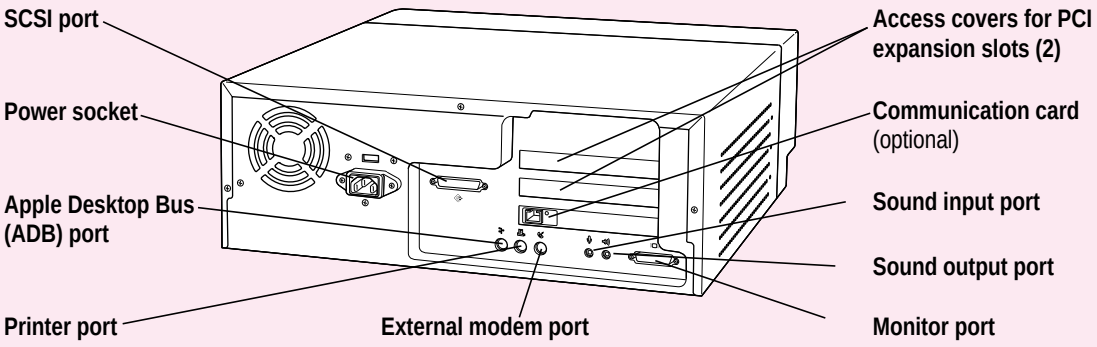


Back View

The back panel includes the power socket, the built-in I/O ports, and the openings for I/O access to the expansion modules: the 2 access covers for PCI I/O expansion cards, and the optional communications card.

Figure 1-2 shows the back view of a Power Macintosh 4400 computer.

Figure 1-2 Back view of the computer



CHAPTER 2

Architecture

This chapter describes the architecture of the Power Macintosh 4400 computer logic board. It describes the major components of the main logic board: the microprocessor, the custom ICs, and the display RAM.

If are already familiar with the Apple Design Logic Board LPX-40, the major differences between the Power Macintosh 4400 computer and the Apple Design Logic Board LPX-40 are:

- the addition of a PCI comm slot on the Power Macintosh 4400 computer 3-slot PCI riser card
- PS/2 ports are not supported
- MFM floppy drive is not supported

Block Diagram and Main ICs

The main logic board of the Power Macintosh 4400 computer uses the PowerPC 603e microprocessor. The board is designed with many of the custom ICs that are used on the Apple Design Logic Board LPX-40. Figure 2-1 shows the system block diagram. The architecture of the main logic board is based on two buses: the processor bus and the PCI bus. The processor bus connects the microprocessor, ROM, cache, and memory; the PCI bus connects the video expansion slots and the I/O devices.

Main Processor

The Power Macintosh 4400 computer has a PowerPC 603e main processor.

PowerPC 603e Microprocessor

The PowerPC 603e microprocessor runs at 200 MHz. The principle features of the PowerPC 603e microprocessor include

- full RISC processing architecture
- parallel processing units: two integer and one floating-point
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- an internal memory management unit (MMU)
- 32 KB of on-chip cache memory (16 KB for data and 16 KB for instructions)

For complete technical details, see the *PowerPC 603 RISC Microprocessor User's Manual.*

Memory Subsystem

The memory subsystem consists of RAM, ROM, and an optional second-level (L2) cache. The PSX custom IC provides burst mode control to the cache and ROM.

RAM

There are no DRAM devices soldered on the logic board. Three slots are provided for RAM expansion. 168-pin 3.3 volt unbuffered EDO (extended data out) JEDEC-standard DRAM DIMM cards are required. The maximum supported DRAM is three slots containing 32 MB each for a total of 96 MB. For additional information about the supported DRAM devices, see “DRAM DIMMs” on page 40.

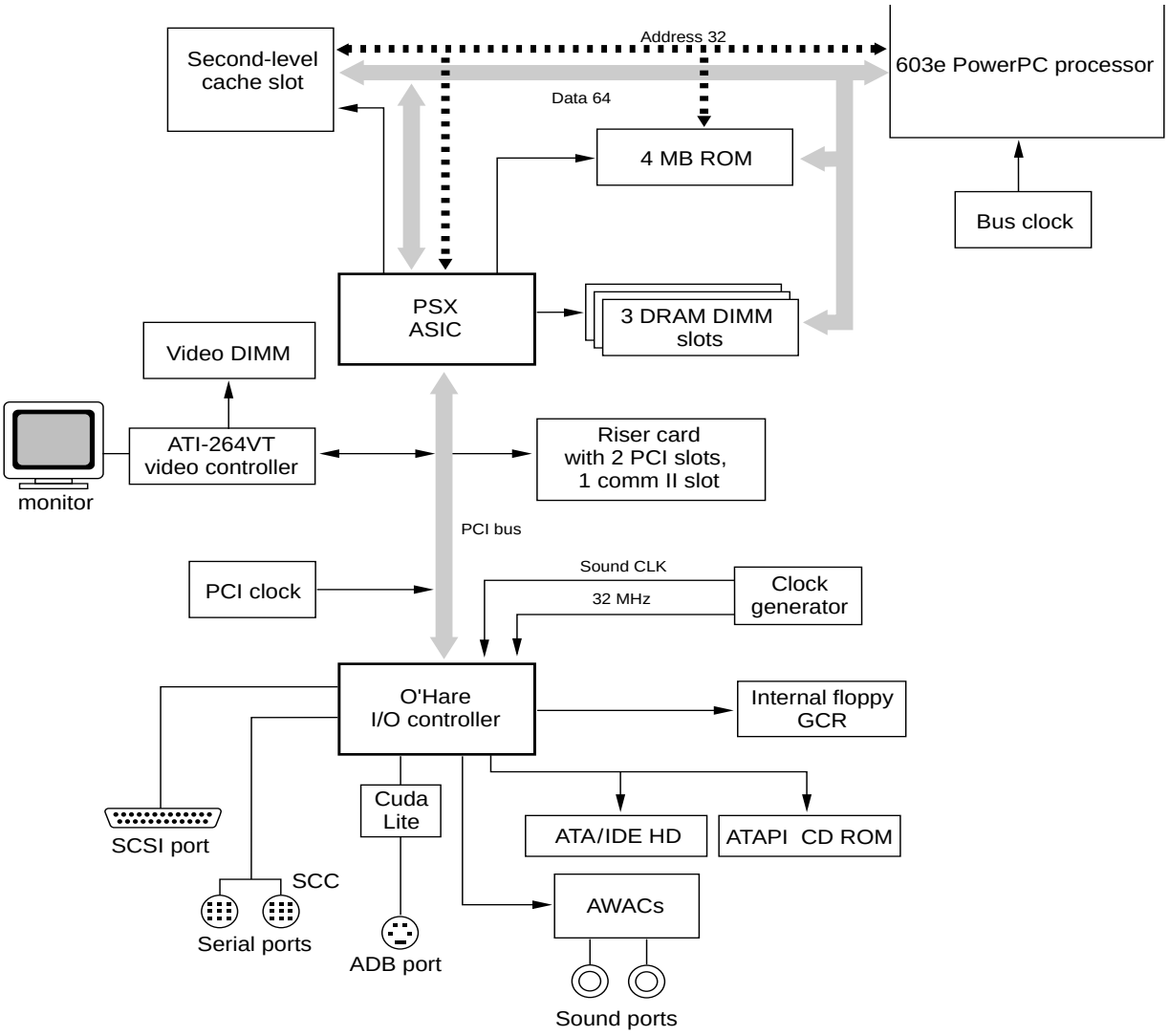
ROM

The ROM consists of 4 MB of masked ROM soldered to the main logic board.

Second-Level Cache (Optional)

The optional second-level (L2) cache consists of 256 KB of high-speed RAM on a 160-pin DIMM card, which is plugged into a 160-pin edge connector on the main logic board. For additional information about the second-level cache, see “Second-Level Cache DIMM” on page 48.

Figure 2-1 System block diagram



System RAM

The Power Macintosh 4400 main logic board has no DRAM memory soldered on the main logic board. All RAM expansion is provided by 3.3 volt unbuffered EDO DRAM devices on 8-byte JEDEC-standard DIMMs. Three 168-pin DIMM sockets are used for memory expansion. Available DRAM DIMM sizes are 8, 16, 32, and 64 MB. DIMM socket 1 supports one-bank DRAM modules. DIMM sockets 2 and 3 support both one- and two-bank DRAM modules. The PSX custom IC provides memory control for the system RAM. For additional information about supported DRAM, see “DRAM DIMMs” beginning on page 40.

Custom ICs

The architecture of the Power Macintosh 4400 main logic board is designed around five large custom integrated circuits:

- the PSX memory controller and PCI bridge
- the O’Hare I/O subsystem and DMA engine
- the AWACS sound processor
- the CudaLite ADB controller
- the ATI 264VT-A4S2 graphics controller

The computer also uses several standard ICs that are used in other Macintosh computers. This section describes only the custom ICs.

PSX IC

The PSX IC functions as the bridge between the PowerPC 603e microprocessor and the PCI bus. It provides buffering and address translation from one bus to the other.

The PSX IC also provides the control and timing signals for system cache, ROM, and RAM. The memory control logic supports byte, word, long word, and burst accesses to the system memory. If an access is not aligned to the appropriate address boundary, PSX generates multiple data transfers on the bus.

Memory Control

The PSX IC controls the system RAM and ROM and provides address multiplexing and refresh signals for the DRAM devices. For information about the address multiplexing, see “RAM Address Multiplexing” on page 45.

PCI Bus Bridge

The PSX IC acts as a bridge between the processor bus and the PCI expansion bus, converting signals on one bus to the equivalent signals on the other bus. The PCI bridge functions are performed by two converters. One converter accepts requests from the processor bus and presents them to the PCI bus. The other converter accepts requests from the PCI bus and provides access to the RAM and ROM on the processor bus.

The PCI bus bridge in the PSX IC runs asynchronously so that the processor bus and the PCI bus can operate at different rates. The processor bus operates at a clock rate of 40 MHz, and the PCI bus operates at 33.33 MHz.

The PCI bus bridge generates PCI parity as required by the PCI bus specification, but it does not check parity or respond to the parity error signal.

Big-Endian and Little-Endian Bus Addressing

Byte order for addressing on the processor bus is big endian and byte order on the PCI bus is little endian. The bus bridge performs the appropriate byte swapping and address transformations to translate between the two addressing conventions. For more information about the translations between big-endian and little-endian byte order, see Part One, "The PCI Bus," in *Designing PCI Cards and Drivers for Power Macintosh Computers.*

Processor Bus to PCI Bus Transactions

Transactions from the processor bus to the PCI bus can be either burst or nonburst. Burst transactions are always 32 bytes long and are aligned on cache-line or 8-byte boundaries. In burst transactions, all the bytes are significant. Burst transactions are used by the microprocessor to read and write large memory structures on PCI devices.

Note
For the processor to generate PCI burst transactions, the address space must be marked as cacheable. Refer to *Macintosh Technote Number 1008, Understanding PCI Bus Performance,* for details. ◆

Nonburst transactions can be of arbitrary length from 1 to 8 bytes and can have any alignment. Nonburst transactions are used by the processor to read and write small data structures on PCI bus devices.

PCI Bus to Processor Bus Transactions

For transactions from the PCI bus to the processor bus, the bridge responds only to PCI bus memory commands and configuration commands. On the processor bus, the bridge generates a burst transaction or a nonburst transaction depending on the type of command and the address alignment. For Memory Write and Invalidate commands that are aligned with the cache line, the bridge generates a burst-write transaction. Similarly, for Memory Read Line and Memory Read Multiple commands whose alignment is less than three-quarters through a cache line, the bridge generates a burst-read transaction. The maximum burst-read or burst-write transaction allowed by the bridge is 32 bytes—8 PCI beats.

Commands other than those mentioned here are limited to two beats if aligned to a processor bus doubleword boundary and to one beat otherwise.

O'Hare IC

The O'Hare IC is based on the Grand Central IC present in the Power Macintosh 7500 computer. It is an I/O controller and DMA engine for Power Macintosh computers using

the PCI bus architecture. It provides power-management control functions for energy management features included on Macintosh computers. The O'Hare IC is connected to the PCI bus and uses the 33.33 MHz PCI bus clock.

The O'Hare IC includes circuitry equivalent to the IDE, SCC, SCSI, sound, SWIM3, and VIA controller ICs. The functional blocks in the O'Hare IC include the following:

- support for descriptor-based DMA for I/O devices
- system-wide interrupt handling
- a SWIM3 floppy drive controller
- SCSI controller (MESH based)
- SCC serial I/O controller
- IDE hard disk interface controller
- sound control logic and buffers

The O'Hare IC provides bus interfaces for the following I/O devices:

- CudaLite ADB controller IC (VIA1 and VIA2 registers)
- AWACS sound input and output IC
- 8 KB nonvolatile RAM control

The SCSI controller in the O'Hare IC is a MESH controller. DMA channels in the O'Hare IC are used to support data transfers. The clock signal to the SCSI controller is 45.1584 MHz.

The O'Hare IC also contains the sound control logic and the sound input and output buffers. There are two DMA data buffers—one for sound input and one for sound output—so the computer can record sound input and process sound output simultaneously. The data buffer contains interleaved right and left channel data for support of stereo sound.

The SCC circuitry in the O'Hare IC is an 8-bit device. The PCLK signal to the SCC is a 24.5 MHz clock. The SCC circuitry supports GeoPort and LocalTalk protocols.

AWACS Sound IC

The audio waveform amplifier and converter (AWACS) is a custom IC that combines a waveform amplifier with a 16-bit digital sound encoder and decoder (codec). It conforms to the IT&T *ASCO 2300 Audio-Stereo Codec Specification* and furnishes high-quality sound input and output. For information about the operation of the AWACS IC, see Chapter 3 of *Developer Note: Power Macintosh Computers,* available on the developer CD-ROM and as part of *Macintosh Developer Note Number 8.*

CudaLite IC

The CudaLite IC is a custom version of the Motorola MC68HC05 microcontroller. It provides several system functions, including

- the ADB interface

- PS2 keyboard and mouse interface
- management of system resets
- management of the real-time clock
- on / off control of the power supply (soft power)

ATI 264VT-A4S2 IC

The ATI 264VT-A4S2 IC is a custom IC containing the logic for the video display. It includes the following functions:

- display memory controller, clock generator, and video DAC (digital-to-analog converter)
- video CLUT (color lookup table)
- 2D graphics acceleration
- true color palette DAC supporting pixel clock rates to 135 MHz for 1280-by-1024 resolution at 75 Hz
- hardware cursor up to 64x64x2
- DCC1 and DDC2B plug-and-play monitor support
- supports EDO DRAM up to 60 MHz memory clock across a 64-bit memory interface
- supports SDRAM or SGRAM up to 80 MHz memory clock, providing a bandwidth up to 640 MB per second

A separate data bus handles data transfers between the ATI 264VT-A4S2 IC and the display memory. The display memory data bus is 64 bits wide for display memory of 2 MB or greater. For 1 MB of display memory, the data bus is 32 bits wide. The ATI 264VT-A4S2 IC breaks each 64-bit data transfer into several pixels of the appropriate size for the current display mode—4, 8, 16, 24, or 32 bits per pixel.

The ATI 264VT-A4S2 IC has an internal phase locked loop (PLL) to generate clocks for the display memory interface and the pixel digital to analog converter (DAC).

The 2D graphics accelerator is a fixed-function accelerator for rectangle fill, line draw, polygon fill, panning / scrolling, bit masking, monochrome expansion, and scissoring with full ROP support.

Display RAM DIMM

The display memory is separate from the main memory. The Power Macintosh 4400 computer supports +5 V EDO DRAM, +3.3 V SDRAM and +3.3 V SGRAM devices for video memory expansion. The video memory DIMM can be configured as 1 MB, 2 MB, or 4 MB.

The maxinmum supported size for an EDO video DIMM is 2 MB. EDO video DIMMs larger than 2 MB provide no additional performance due to the limited bandwidth of the EDO devices.

With a 4 MB SGRAM DIMM, the display data generated by the computer can have pixel depths of 4, 8, 16, 24, or 32 bits for monitors up to 1024-by-768 pixels and 4, 8, or 16 bits for larger monitors up to 1280-by-1024 pixels.

For additional information about video on the Power Macintosh 4400 main logic board, see “Built-in Video” on page 34 and “Video RAM” on page 50.

CHAPTER 3

I/O Features

This chapter describes both the built-in I/O devices and the interfaces for external I/O devices. It also describes the types of external video monitors that can be used with the Power Macintosh 4400 computer.

Board Layout

The Power Macintosh 4400 logic board is built to the industry standard LPX 13-by-9 inch form factor. The layout of the connectors on the board is shown in Figure 3-1.

Figure 3-1 Power Macintosh 4400 connector layout

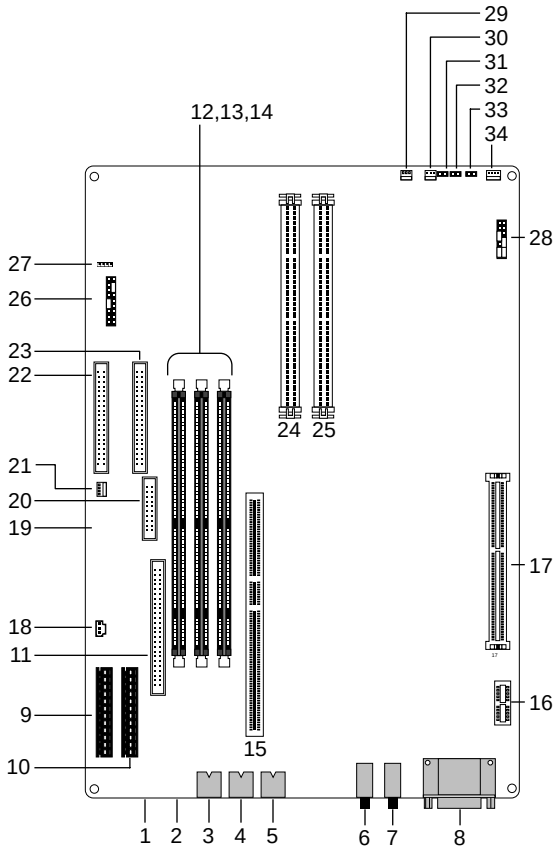


Table 3-1 lists the locations and types of connectors on the Power Macintosh 4400 logic board. Refer to the connector numbers in Figure 3-1 to determine the location of each connector on the logic board.

Table 3-1 Connectors on the Power Macintosh 4400 logic board

Location	Description	Connector type
1	PS/2 mouse port	6-pin mini-DIN (not on Power Macintosh 4400 logic board)
2	PS/2 keyboard port	6-pin mini-DIN (not on Power Macintosh 4400 logic board)
3	Apple ADB port	4-pin mini-DIN
4	Apple printer serial port	9-pin mini-DIN
5	Apple modem serial port	9-pin mini-DIN
6	Sound in	Mini-phono jack
7	Sound out	Mini-phono jack
8	Monitor out	15-pin Macintosh
9	Power supply	12-pin header
10	Power supply	12-pin header
11	SCSI	50-pin header
12	DRAM DIMM slot 3	168-pin connector
13	DRAM DIMM slot 2	168-pin connector
14	DRAM DIMM slot 1	168-pin connector
15	PCI riser connector	192-pin connector
16	GIMO	22-pin connector
17	Video DIMM	120-pin connector
18	Power supply soft power	3-pin header
19	MFM floppy disk drive	34-pin header (not on Power Macintosh 4400 logic board)
20	Apple GCR floppy disk drive	20-pin header
21	CD-audio	4-pin header
22	ATAPI CD-ROM	40-pin header
23	ATA (IDE) hard disk	40-pin header
24	ROM connector	160-pin connector
25	L2 cache connector	160-pin connector

continued

Table 3-1 Connectors on the Power Macintosh 4400 logic board (continued)

Location	Description	Connector type
26	Feature options jumper	(6) 3-pin headers
27	Battery connector	4-pin header
28	CPU frequency multiplier (jumper)	(4) 3-pin headers
29	Fan	3-pin header
30	Power LED	3-pin header
31	Reset switch	2-pin header
32	Soft power switch	2-pin header
33	NMI switch	2-pin header
34	Speaker	4-pin header

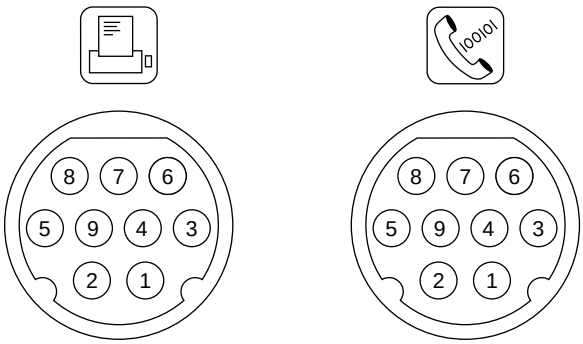
Serial I/O Ports

The Power Macintosh 4400 computer has two standard Macintosh serial ports: two 9-pin mini-DIN serial ports for a printer and a modem.

Apple Printer and Modem Ports

The printer and modem serial ports have 9-pin mini-DIN sockets that accept either 8-pin or 9-pin plugs. Both ports support LocalTalk and GeoPort serial protocols. Figure 3-2 shows the mechanical arrangement of the pins on the serial port sockets; Table 3-2 shows the signal assignments.

Figure 3-2 Serial port sockets



Printer Modem

Table 3-2 Serial port signals

Pin	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input (external clock on modem port)
3	TxD–	Transmit data –
4	GND	Ground
5	RxD–	Receive data –
6	TxD+	Transmit data +
7	GPi	General-purpose input (wakeup CPU or perform DMA handshake)
8	RxD+	Receive data +
9	+5 V	+5 volts to external device (100 mA maximum)

Note
Pin 9 on each serial connector provides +5 V power for external devices. The total current available for all devices connected to the +5 V pins on the serial ports and ADB ports is 500 mA. Each external device should draw no more than 100 mA. Excessive current drain will cause a fuse to interrupt the +5 V supply; the fuse automatically resets when the load returns to normal. ◆

Both serial ports include the GPi (general-purpose input) signal on pin 7. The GPi signal for each port connects to the corresponding data carrier detect input on the SCC portion of the O'Hare custom IC, described in Chapter 2. On both serial ports, the GPi line can be connected to the receive / transmit clock (RTxCA) signal on the SCC. That connection supports devices that provide separate transmit and receive data clocks, such as

synchronous modems. For more information about the serial ports, see *Guide to the Macintosh Family Hardware*, second edition.

ADB Port

The Apple Desktop Bus (ADB) port on the Power Macintosh 4400 computer is functionally the same as on other Macintosh computers.

The ADB is a single-master, multiple-slave serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin mini-DIN connector connects the ADB to the external devices. Table 3-3 lists the ADB connector pin assignments. For more information about the ADB, see *Guide to the Macintosh Family Hardware*, second edition.

Table 3-3 ADB connector pin assignments

Pin	Signal name	Description
1	ADB	Bidirectional data bus used for input and output. It is an open-collector signal pulled up to +5 volts through a 470-ohm resistor on the main logic board.
2	PSW	Power-on / off signal.
3	+5 V	+5 volts to external device.
4	GND	Ground.

Note
The total current available for all devices connected to the +5 V pins on the ADB, Macintosh serial ports is a maximum of 500 mA. Each device should use no more than 100 mA. ◆

Apple ADB Keyboard

The Apple ADB keyboard has a Power key, identified by the symbol ⏻. Pressing the Power key button will turn on the computer. When the user chooses Shut Down from the Special menu, the computer either shuts down or a dialog box appears asking if you really want to shut down. The user can also turn off the power by pressing the Power key.

Enclosures may or may not include a programmer’s switch to reset the computer. If an enclosure does not have a programmer’s switch, the user invokes the reset and nonmaskable interrupt (NMI) functions by pressing Command key combinations while

holding down the Power key, as shown in Table 3-4. The Command key is identified by the symbols ⌘ and X.

Note
The user must hold down a key combination for at least 1 second to allow the ADB microcontroller enough time to respond to the NMI or hard-reset signal. ◆

Table 3-4 Reset and NMI key combinations

Key combination	Function
Command-Power (x-p)	NMI (always active)
Control-Command-Power (Control-x-p)	Reset

Disk Drives

The Power Macintosh 4400 computer has a connector for one GCR (group code recording) internal high-density floppy disk drive, one internal ATA (IDE) hard disk drive, an internal ATAPI CD-ROM drive, and external SCSI devices.

Floppy Disk Drives

The Power Macintosh 4400 has connectors for either a GCR or MFM floppy disk drive. The GCR connector is for an internal high-density floppy disk drive (Apple SuperDrive). The MFM connector is for an internal high-density MFM floppy disk drive.

GCR Floppy Disk Drive

The GCR drive is connected with a 20-pin cable that is connected to the main logic board. Table 3-5 shows the pin assignments on the GCR floppy disk connector.

Table 3-5 Pin assignments on the GCR floppy disk connector

Pin	Signal name	Description
1	GND	Ground
2	PH0	Phase 0: state control line
3	GND	Ground
4	PH1	Phase 1: state control line

continued

Table 3-5 Pin assignments on the GCR floppy disk connector (continued)

Pin	Signal name	Description
5	GND	Ground
6	PH2	Phase 2: state control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	+5 V	+5 volts
10	/WRREQ	Write data request
11	+5 V	+5 volts
12	SEL	Head select
13	+12 V	+12 volts
14	/ENBL	Drive enable
15	+12 V	+12 volts
16	RD	Read data
17	+12 V	+12 volts
18	WR	Write data
19	+12 V	+12 volts
20	n.c.	Not connected

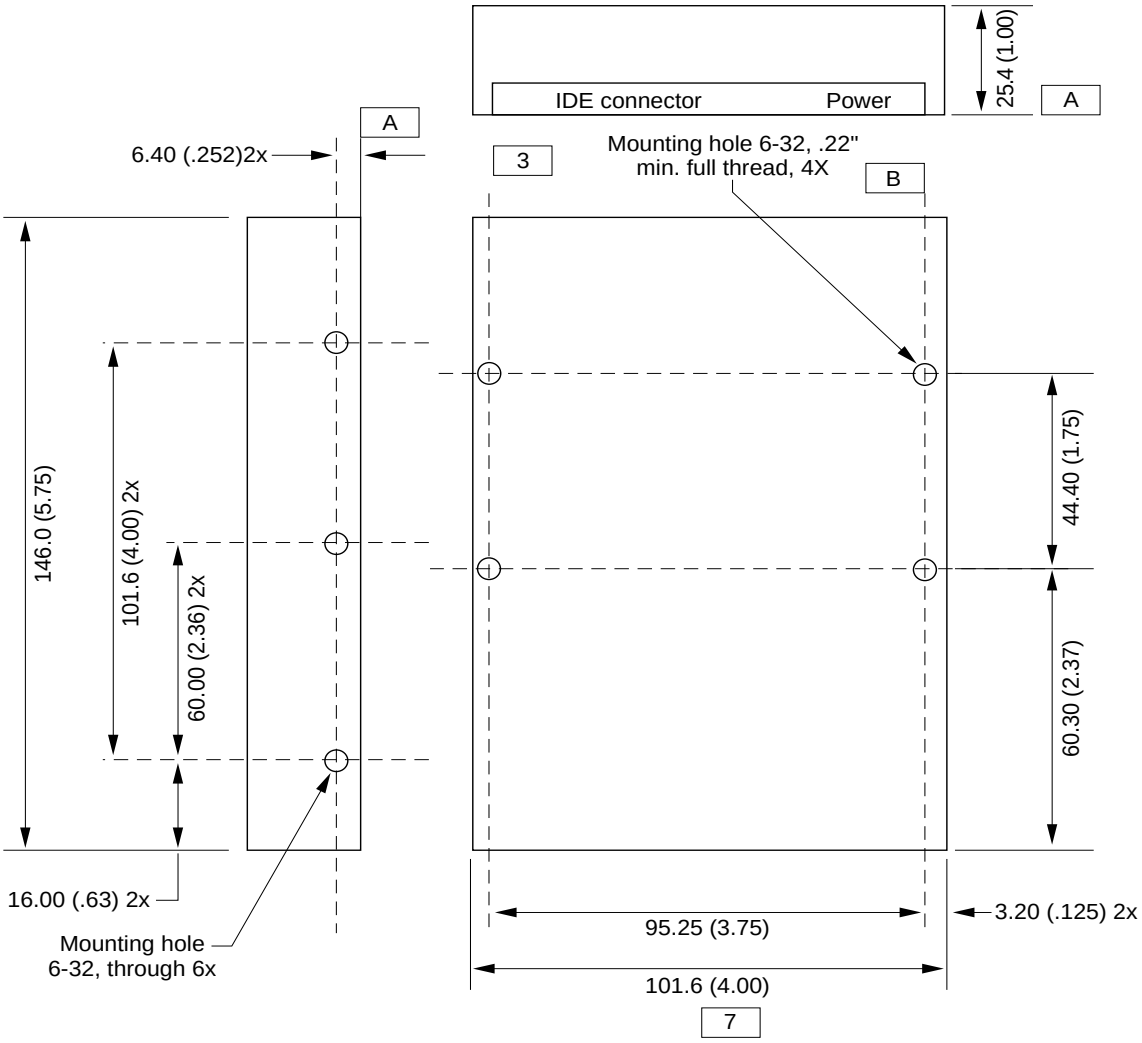
ATA (IDE) Hard Disk

The Power Macintosh 4400 computer has an internal hard disk that complies with the standard ATA-3 interface. This interface, used for ATA drives on IBM AT–compatible computers, is also referred to as the IDE interface. The hard drives used on the Power Macintosh 4400 computer must have software drivers and hardware termination that comply with revision 3.1 of the ATA-3 interface specification.

Hard Disk Specifications

Figure 3-3 shows the maximum dimensions of the hard disk and the location of the mounting holes. As the figure shows, the minimum clearance between conductive components and the bottom of the mounting envelope is 0.5 mm.

Figure 3-3 Maximum dimensions of the hard disk



Notes:

1 A Defined by plane of bottom mount holes

2 B Defined by center line of bottom mount holes

3 40-pin IDE and 4-pin power connector placement must not be reversed

4 Dimensions are in millimeters (inches)

5 Drawing not to scale

6 Tolerances .X = ±0.50, .XX = ±0.25

7 Dimension to be measured at center line of side-mount holes

8 Minimum 0.5 MM clearance from any conductive PCB components to A

Hard Disk Connectors

The internal hard disk has a standard 40-pin ATA connector and a separate 4-pin power connector.

The exact locations of the ATA connector and the power connector are not specified, but the relative positions must be as shown in Figure 3-3 so that the cables and connectors will fit.

Pin Assignments

Table 3-6 shows the pin assignments on the 40-pin ATA (IDE) hard disk connector. A slash (/) at the beginning of a signal name indicates an active-low signal.

Table 3-6 Pin assignments on the ATA (IDE) hard disk connector

Pin number	Signal name	Pin number	Signal name
1	/RESET	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	Key
21	DMA_REQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	/IORDY	28	Reserved
29	DMA_ACK	30	GROUND
31	INTRQ	32	/IOCS16
33	DA1	34	/PDIAG (not connected)
35	DA0	36	DA2
37	/CS0	38	/CS1
39	/DASP (not connected)	40	GROUND

ATA (IDE) Signal Descriptions

Table 3-7 describes the signals on the ATA (IDE) hard disk connector.

Table 3-7 Signals on the ATA (IDE) hard disk connector

Signal name	Signal description
DA(0–2)	ATA device address; used by the computer to select one of the registers in the ATA drive. For more information, see the descriptions of the CS0 and CS1 signals.
DD(0–15)	DD(0–15) are used to transfer 16-bit data to and from the drive buffer. DD(8–15) are used to transfer data to and from the internal registers of the drive, with DD(0–7) driven high when writing.
DMA_REQ	DMA request.
DMA_ACK	DMA acknowledge.
/CS0	ATA register select signal. It is asserted high to select the additional control and status registers on the ATA drive.
/CS1	ATA register select signal. It is asserted high to select the main task file registers. The task file registers indicate the command, the sector address, and the sector count.
/IORDY	ATA I/O ready; when driven low by the drive, signals the CPU to insert wait states into the I/O read or write cycles.
/IOCS16	ATA I/O channel select; asserted low for an access to the data port. The computer uses this signal to indicate a 16-bit data transfer.
DIOR	ATA I/O data read strobe.
DIOW	ATA I/O data write strobe.
INTRQ	ATA interrupt request. This active-high signal is used to inform the computer that a data transfer is requested or that a command has terminated.
/RESET	Hardware reset to the drive; an active-low signal.
Key	This pin is the key for the connector.

CD-ROM Drive

The Power Macintosh 4400 logic board has a connector for an internal ATAPI CD-ROM drive. The CD-ROM software supports the worldwide standards and specifications for CD-ROM and CD-digital audio discs described in the Sony/Philips Yellow Book and Red Book. The drive can read CD-ROM, CD-ROM XA, CD-I, and PhotoCD discs as well as play standard audio discs.

The ATA (IDE) hard drive and ATAPI CD-ROM drive are both master devices on the same data bus. Slave ATA (IDE) devices are not supported.

The pin assignments for the ATAPI CD-ROM drive connector are identical to those listed in Table 3-7 for the ATA hard disk drive connector.

SCSI Bus

The Power Macintosh 4400 logic board has a SCSI bus for external SCSI devices.

SCSI Connector

The SCSI connector is a 50-pin connector with the standard SCSI pin assignments. The external SCSI connector is a 25-pin D-type connector with the same pin assignments as other Apple SCSI devices. Table 3-8 shows the pin assignments on the internal and external SCSI connectors.

Table 3-8 Pin assignments for the SCSI connectors

Pin number (internal 50-pin)	Pin number (external 25-pin)	Signal name	Signal description
2	8	/DB0	Bit 0 of SCSI data bus
4	21	/DB1	Bit 1 of SCSI data bus
6	22	/DB2	Bit 2 of SCSI data bus
8	10	/DB3	Bit 3 of SCSI data bus
10	23	/DB4	Bit 4 of SCSI data bus
12	11	/DB5	Bit 5 of SCSI data bus
14	12	/DB6	Bit 6 of SCSI data bus
16	13	/DB7	Bit 7 of SCSI data bus
18	20	/DBP	Parity bit of SCSI data bus
25	–	n.c.	Not connected
26	25	TPWR	+5 V terminator power
32	17	/ATN	Attention
36	6	/BSY	Bus busy
38	5	/ACK	Handshake acknowledge
40	4	/RST	Bus reset
42	2	/MSG	Message phase
44	19	/SEL	Select
46	15	/C/D	Control or data

continued

Table 3-8 Pin assignments for the SCSI connectors (continued)

Pin number (internal 50-pin)	Pin number (external 25-pin)	Signal name	Signal description
48	1	/REQ	Handshake request
50	3	/I/O	Input or output
20, 22, 30, 34, and all odd pins except pins 23, 25, and 27	7, 9, 14, 16, 18, and 24	GND	Ground

SCSI Bus Termination

The SCSI bus is terminated internally by a passive terminator. The terminator is located on the main logic board near the SCSI connector.

Sound

The sound system supports both 8-bit and 16-bit stereo sound output and input.

The Power Macintosh 4400 computer can create sounds digitally and play the sounds through the internal speaker or send the sound signals out through the sound-output jack. The Power Macintosh 4400 computer also records sound from several sources: a microphone or other sound-intput source connected to the sound-input jack or a compact disc in the CD-ROM player. With each sound-input source, sound playthrough can be enabled or disabled.

Sound Output

The Power Macintosh 4400 computer has a connector at the front of the logic board for built-in speaker support and one sound-output jack at the back of the board. The rear jack is intended for use with external speakers or headphones. The sound-output jack is a stereophonic mini-phono jack. Table 3-9 lists the signal assignments for the sound-output jack.

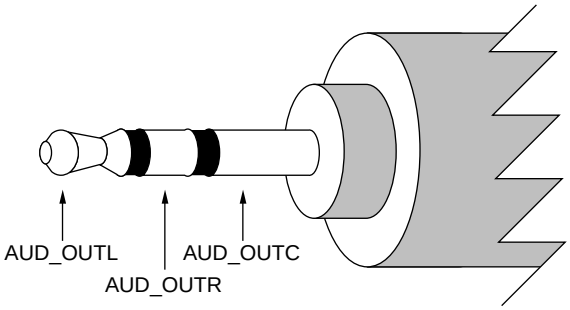
Sound output is controlled by the O'Hare IC. The AWACS IC provides the stereo sound-output to both the internal speaker and the sound-output jacks.

Table 3-9 Signal assignments for the sound output connector

Pin	Signal name	Description
1	AUD_OUTC	Audio-output common
2	AUD_OUTL	Audio-output left channel
3	AUD_OUTS	Audio-output sense
4	AUD_OUTR	Audio-output right channel
5	n.c.	Not connected
6	Shield	Shield
7	Shield	Shield
8	Shield	Shield

The mini-phono jack for the sound-output port should be wired as shown in Figure 3-4.

Figure 3-4 Mini-phono jack for sound output



Sound Input

The Power Macintosh 4400 computer has a stereo sound-input jack on the back for connecting an external microphone or other sound source. The sound-input jack accepts a standard 1/8-inch stereophonic phone plug (two signals plus ground).

The sound-input jack accepts either the Apple PlainTalk line-level microphone or a pair of line-level signals.

Note
The Apple PlainTalk microphone requires power from the main computer, which it obtains by way of an extra-long, 4-conductor plug that makes contact with a 5-volt pin inside the sound-input jack. ◆

IMPORTANT
The microphone for the Macintosh LC and LC II does not work with the Power Macintosh 4400 computer; it requires the line-level signal provided by the Apple PlainTalk microphone. ▲

The available current allowance for the microphone on +5 V is 20 mA.

Sound Input Specifications

The sound input jack has the following electrical characteristics:

- input impedance: 15k ohms
- maximum input level: 1.06 V RMS

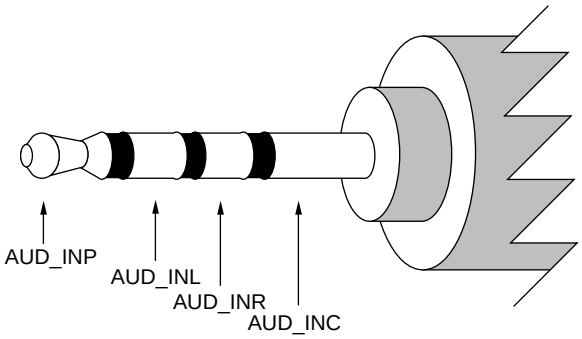
Table 3-10 lists the signal assignments for the sound-input jack.

Table 3-10 Signal assignments for the sound-nput jack

Pin	Signal name	Description
1	AUD_INC	Audio-input common
2	AUD_INL	Audio-input left channel
3	AUD_IN_SENSE	Audio-input sense
4	AUD_INR	Audio-input right channel
5	n.c.	Not connected
6	Shield	Shield
7	Shield	Shield
8	Shield	Shield
9	AUD_INP	Audio microphone +5 V power less than 20 mA
10	MIC_SENSE	Audio microphone sense

Figure 3-5 shows how a PlainTalk compatible mini-phono microphone sound-input jack should be wired.

Figure 3-5 Mini-phono microphone sound-input jack



Digitizing Sound

The Power Macintosh 4400 computer digitizes and records sound as 16-bit samples. The computer can use one of three sampling rates: 11k samples per second, 22k samples per second, and 44k samples per second.

The sound system plays samples at the sampling rate specified in the control panel for sound.

Sound Modes

The sound mode is selected by a call to the Sound Manager. The sound circuitry normally operates in one of three modes:

- Sound playback: computer-generated sound is sent to the speaker and the sound-output jacks.
- Sound playback with playthrough: computer sound and sound input are mixed and sent to the speakers and the sound-output jacks.
- Sound record with playthrough: input sound is recorded and also fed through to the speakers and the sound-output jacks.

When recording from a microphone, applications should reduce the playthrough volume to prevent possible feedback from the speakers to the microphone.

The O’Hare IC provides separate sound buffers for input and for stereo output, so the computer can record and send digitized sound to the sound outputs simultaneously.

Built-in Video

The built-in video circuitry supports pixel display sizes of 512 by 384, 640 by 480, 800 by 600, 832 by 624, 1024 by 768, 1152 by 870, 1280 by 960, and 1280 by 1024. When power is applied, the monitor is initially set for a display size of 640-by-480 pixels. With a multisync monitor the user can switch the monitor resolution on the fly from the

Monitor bit depth and resolution modules in the Control Strip or from the Monitors and Sound control panel.

Video Connector

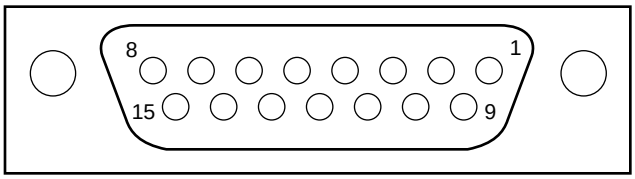
The Power Macintosh 4400 computer has a standard Macintosh 15-pin monitor connector. The pin assignments for the Macintosh 15-pin external monitor connector on the Power Macintosh 4400 computer are shown in Table 3-11.

Table 3-11 Pin assignments for the Macintosh 15-pin external monitor connector

Pin number	Signal name	Description
1	RED Return	Red video ground
2	RED	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Apple monitor sense signal 0
5	GREEN	Green video signal
6	GREEN Return	Green video ground
7	SENSE1 (SCL)	Apple monitor sense signal 1 (DDC clock)
9	BLUE	Blue video signal
10	SENSE2 (SDA)	Apple monitor sense signal 2 (DDC clock)
11	GND	CSYNC and VSYNC ground
12	/VSYNC	Vertical synchronization signal
13	BLUE Return	Blue video ground
14	GND	HSYNC ground
15	/HSYNC	Horizontal synchronization signal

Figure 3-6 shows the physical pinout for the Macintosh 15-pin external monitor connector.

Figure 3-6 Macintosh 15-pin external monitor connector



Video Display Sense Codes

The Power Macintosh 4400 computer supports both Apple and PC compatible monitors. Apple monitors currently use a 15-pin connector that has three signals that are sensed to determine which monitor is connected. The ability to sense the monitor is important, because it makes it possible for the computer to establish a valid video display screen for the user at boot time without any additional user input.

PC compatible monitors use a high density 15-pin SVGA connector that has four pins used for sense signals. The 4-pin sensing scheme has unfortunately been largely ignored and a new video display sensing scheme, referred to as DDC, is used to replace the 4-bit sense code. The DDC (display data channel) sensing scheme uses a serial bit stream from the monitor to determine which resolutions are valid and available.

The monitor sensing sequence for the Macintosh 15-pin configuration is as follows:

1. The DDC sense code is checked. If a valid code is found, sensing is complete.
2. The Apple monitor sense codes are checked. If a valid code is found, sensing is complete.
3. If a load is found on the RGB lines, then a VGA monitor is assumed to be connected and 640-by-480 pixel resolution at 60 Hz is displayed.
4. If no load is found, then video is not displayed.

For every valid sense code, there is a default display mode chosen the first time the computer is started with a monitor attached. The user may change the default display mode to one of the other supported modes, and the system will use the new display mode the next time it is started or returns from a reset with the same monitor attached. If the monitor is switched before the next time the system is started, the default display mode is again chosen. Table 3-12 lists the sense codes, default display modes, valid display modes, and safe display modes for several monitors.

Table 3-12 Video display sense codes

Monitor	Sense code (hex)	Default display mode	Valid display modes	Safe display modes
13-inch color	06 2B	640 x 480	640 x 480	640 x 480
16-inch color	07 2D	832 x 624	832 x 624	832 x 624
19-inch RGB	07 3A	1024 x 768	1024 x 768	1024 x 768
21-inch color two-page	00 XX / 03 XX	1152 x 870	1152 x 870	1152 x 870
Apple MultiScan 14/15-inch	06 03	640 x 480	640 x 480, 800 x 600, 832 x 624, 1024 x 768	640 x 480, 800 x 600, 832 x 624

continued

Table 3-12 Video display sense codes

Monitor	Sense code (hex)	Default display mode	Valid display modes	Safe display modes
Apple MultiScan 1705	06 0B	832 x 624	640 x 480, 800 x 600, 832 x 624, 1024 x 768	640 x 480, 800 x 600, 832 x 624, 1024 x 768
Apple MultiScan 20-inch	06 23	1152 x 870	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024
AppleVision 1710	06 2B	640 x 480	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024
VGA / VESA	07 17	640 x 480	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480

Video Display Resolution

The Power Macintosh 4400 computer supports several display resolution sizes for external video monitors. Table 3-13 shows the display resolutions supported and the maximum pixel depths available for a given amount of video memory. The maximum pixel depth available depends on the monitor's screen resolution setting and the amount of video RAM installed.

Table 3-13 Maximum pixel depths for resolution setting

Display resolution, in pixels	Vertical refresh, Hz	Horizontal refresh, kHz	Pixel clock, MHz	Maximum pixel depth, in bits per pixel EDO DRAM		Maximum pixel depth, in bits per pixel SGRAM or SDRAM	
				1 MB	2 MB	2 MB	4 MB
512 x 384	70.130	31.488	21.160	16	32	32	32
640 x 480	59.940	31.469	25.175	16	32	32	32
640 x 480	66.667	35.000	30.240	16	32	32	32
640 x 480	72.809	37.861	31.500	16	32	32	32
640 x 480	75.000	37.500	31.500	16	32	32	32
640 x 870	75.000	68.850	57.283	8	16	16	32
800 x 600	60.317	37.879	40.000	16	32	32	32
800 x 600	72.188	48.077	50.000	16	32	32	32
800 x 600	75.000	46.875	49.500	16	16	32	32
832 x 624	74.500	49.725	57.283	16	16	32	32
1024 x 768	60.004	48.363	65.000	8	16	16	32
1024 x 768	70.069	56.476	75.000	8	16	16	32
1024 x 768	75.029	60.023	78.750	8	16	16	32
1152 x 870	75.062	68.681	100.000	8	16	16	16
1280 x 960	75.000	75.000	126.000	na	8	8	16
1280 x 1024	60.020	63.981	108.000	na	8	8	16
1280 x 1024	75.025	79.976	135.000	na	8	8	16

CHAPTER 4

Expansion Features

This chapter describes the expansion features supported on the Power Macintosh 4400 computer logic board: the DRAM expansion slots, the L2 cache expansion slot, and the PCI expansion slots.

Note
Apple does not support development of third-party second-level (L2) cache cards, because the L2 cache controller is integrated into the design of the cache card. ◆

DRAM DIMMs

The Power Macintosh 4400 computer logic board has three DRAM expansion slots. The DRAM expansion slots accept 3.3 volt EDO unbuffered (extended data output) 8-byte DIMMs (dual inline memory modules). As its name implies, the 8-byte DIMM has a 64-bit-wide data bus.

The DRAM DIMM is an industry standard memory module. Its mechanical design is defined by the JEDEC MO-161 specification. The DRAM DIMM connector used on the logic board is Hon Hai's Precision / Foxconn part number AT08417-V8 or equivalent.

The Power Macintosh 4400 computer logic board supports five banks of memory. DIMM slot 1 supports only single-bank DIMMs. DRAM expansion slots 2 and 3 support both one and two-bank DIMMs. The maximum amount of memory supported on the Power Macintosh 4400 computer logic board is one 32 MB DIMM (slot 1) and two 64 MB DIMMs (slots 2 and 3), for a total of 160 MB.

The minimum bank size supported by the PSX IC is 4 MB and the largest is 64 MB; the largest DIMM supported is a two-bank DIMM holding 64 MB. Table 4-1 shows the single-bank DRAM DIMM configurations supported in DIMM slot 1 on the Power Macintosh 4400 computer logic board.

Table 4-1 DRAM DIMM configurations supported in DIMM slot 1

DIMM size	Device technology	Width	Quantity
8 MB	4 Mbit	1 Mbits x 4	16
8 MB	16 Mbit	1 Mbits x 16	4
16 MB	16 Mbit	2 Mbits x 8	8
32 MB	16 Mbit	4 Mbits x 4	16
32 MB	64 Mbit	4 Mbits x 16	4

IMPORTANT

The number of DRAM devices on a DRAM DIMM is constrained by the load limits of the unbuffered signals. A maximum of two devices can be connected to each data line, a maximum of eight devices can be connected to each /RAS or /CAS line, and a maximum of sixteen devices can be connected to each address line. This limits a DIMM to 32 MB using 16-megabit DRAM devices. ▲

Table 4-2 shows the one and dual-bank DRAM DIMM configurations supported in DIMM slots 2 and 3 on the Power Macintosh 4400 computer logic board.

Table 4-2 DRAM DIMM configurations supported in DIMM slots 2 and 3

DIMM size	Device technology	Width	Quantity	Banks
8 MB	4 Mbit	1 Mbits x 4	16	2
8 MB	16 Mbits	1 Mbits x 16	4	1
16 MB	16 Mbits	2 Mbits x 8	8	1
16 MB	16 Mbits	1 Mbits x 16	8	2
32 MB	16 Mbits	4 Mbits x 4	16	1
64 MB	16 Mbits	4 Mbits x 4	32	2
32 MB	16 Mbits	2 Mbits x 8	16	2
32 MB	64 Mbits	4 Mbits x 16	4	1
64 MB	64 Mbits	4 Mbits x 16	8	2

IMPORTANT

The PSX DRAM controller on the Power Macintosh 4400 computer logic board does not provide support for 4 M by 4 bits with 12 by 10 addressing or 1 M by 16 bits with 12 by 8 or with 11-by-9 addressing DRAM devices. ▲

The only 64-megabit DRAM devices supported on the Power Macintosh 4400 logic board must be configured as 4 M by 16 bits with 11-by-11 row and column addressing (not 12 by 10 addressing). Devices configured as 8 M by 8 bits or 16 M by 4 bits will not work, because the maximum memory addressed by a bank is 32 MB.

The DRAM DIMMs can be installed one or more at a time. The Power Macintosh 4400 computer supports only linear memory organization, therefore no performance gains are seen when two DIMMs of the same size are installed. Any size DIMM can be installed in the three DIMM slots, and the combined memory of all of the DIMMs installed will be configured as a contiguous memory space.

DRAM DIMM Connectors

Table 4-3 gives the pin assignments for the 168-pin 3.3 V unbuffered EDO DRAM DIMM connectors.

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors

Pin number	Signal name	Pin number	Signal name
1	GND	85	GND
2	D(0)	86	D(32)
3	D(1)	87	D(33)
4	D(2)	88	D(34)
5	D(3)	89	D(35)
6	+3.3 V	90	+3.3 V
7	D(4)	91	D(36)
8	D(5)	92	D(37)
9	D(6)	93	D(38)
10	D(7)	94	D(39)
11	D(8)	95	D(40)
12	GND	96	GND
13	D(9)	97	D(41)
14	D(10)	98	D(42)
15	D(11)	99	D(43)
16	D(12)	100	D(44)
17	D(13)	101	D(45)
18	+3.3 V	102	+3.3 V
19	D(14)	103	D(46)
20	D(15)	104	D(47)
21	Reserved	105	Reserved
22	Reserved	106	Reserved
23	GND	107	GND
24	Reserved	108	Reserved
25	Reserved	109	Reserved
26	+3.3 V	110	+3.3 V
27	/WE(0)	111	Reserved

continued

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors (continued)

Pin number	Signal name	Pin number	Signal name
28	/CAS(0)	112	/CAS(4)
29	/CAS(1)	113	/CAS(5)
30	/RAS(0)	114	/RAS(2)
31	/OE(0)	115	Reserved
32	GND	116	GND
33	A(0)	117	A(1)
34	A(2)	118	A(3)
35	A(4)	119	A(5)
36	A(6)	120	A(7)
37	A(8)	121	A(9)
38	A(10)	122	A(11)
39	Not used	123	Not used
40	+3.3 V	124	+3.3 V
41	+3.3 V	125	Reserved
42	Reserved	126	Reserved
43	GND	127	GND
44	/OE(2)	128	Reserved
45	/RAS(1)	129	/RAS(3)
46	/CAS(2)	130	/CAS(6)
47	/CAS(3)	131	/CAS(4)
48	/WE(2)	132	Reserved
49	+3.3 V	133	+3.3 V
50	Not used	134	Not used
51	Not used	135	Not used
52	Not used	136	Not used
53	Not used	137	Not used
54	GND	138	GND
55	D(16)	139	D(48)
56	D(17)	140	D(49)
57	D(18)	141	D(50)
58	D(19)	142	D(51)

continued

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors (continued)

Pin number	Signal name	Pin number	Signal name
59	+3.3 V	143	+3.3 V
60	D(20)	144	D(52)
61	Not used	145	Not used
62	Not used	146	Not used
63	Not used	147	Not used
64	GND	148	GND
65	D(21)	149	D(53)
66	D(22)	150	D(54)
67	D(23)	151	D(55)
68	GND	152	GND
69	D(24)	153	D(56)
70	D(25)	154	D(57)
71	D(26)	155	D(58)
72	D(27)	156	D(59)
73	+3.3 V	157	+3.3 V
74	D(28)	158	D(60)
75	D(29)	159	D(61)
76	D(30)	160	D(62)
77	D(31)	161	D(63)
78	GND	162	GND
79	Not used	163	Not used
80	Not used	164	Not used
81	Not used	165	Not used
82	Not used	166	Not used
83	Not used	167	Not used
84	+3.3 V	168	+3.3 V

Table 4-4 describes the signals on the RAM DIMM connector.

Table 4-4 RAM DIMM signals

Signal name	Description
A(11:0)	Address inputs
/CAS(7:0)	Column address strobe signals
D(63:0)	Data input and output signals
/OE(0, 2)	Output enable signals
/RAS(3:0)	Row address strobe signals
Reserved	Reserved, don't use
+3.3V	+3.3 V power
GND	Ground (VSS)
/WE(0, 2)	Read/write input signals

RAM Address Multiplexing

Signals A[11:0] on each RAM DIMM make up a 12-bit multiplexed address bus that can support several different types of DRAM devices. Table 4-5 shows the address multiplexing modes used with several types of DRAM devices. The devices are characterized by their bit dimensions: for example, a 4 M by 4-bit device has 4-M addresses and stores 4 bits at a time.

Table 4-5 Address multiplexing modes for various DRAM devices

Device size	Device type	Size of row address	Size of column address
4 Mbits	1 M by 4 bits	10	10
16 Mbits	1 M by 16 bits	10	10
16 Mbits	2 M by 8 bits	11	10
16 Mbits	2 M by 8 bits	12	9
16 Mbits	4 M by 4 bits	11	11

Table 4-6 shows how the address signals to the RAM devices are multiplexed during the row and column address phases for noninterleaved banks.

Table 4-6 Address multiplexing in noninterleaved banks

	Individual signals on the DRAM_ADDR bus											
	A(11)	**A(10)**	**A(9)**	**A(8)**	**A(7)**	**A(6)**	**A(5)**	**A(4)**	**A(3)**	**A(2)**	**A(1)**	**A(0)**
Row address	22	23	21	20	19	18	17	16	15	14	13	12
Column address		24	22	11	10	9	8	7	6	5	4	3

RAM Devices

The memory controller in the PSX IC supports 4 Mbit and 16 Mbit 3.3 V unbuffered EDO DRAM devices. The access time (T_{RAS}) of the DRAM devices is 60 ns or faster.

RAM Refresh

The PSX IC provides a CAS-before-RAS refresh cycle every 15.6 µs. DRAM devices must be compatible with this refresh cycle; for example, this cycle will refresh 2K-refresh parts within 32 milliseconds.

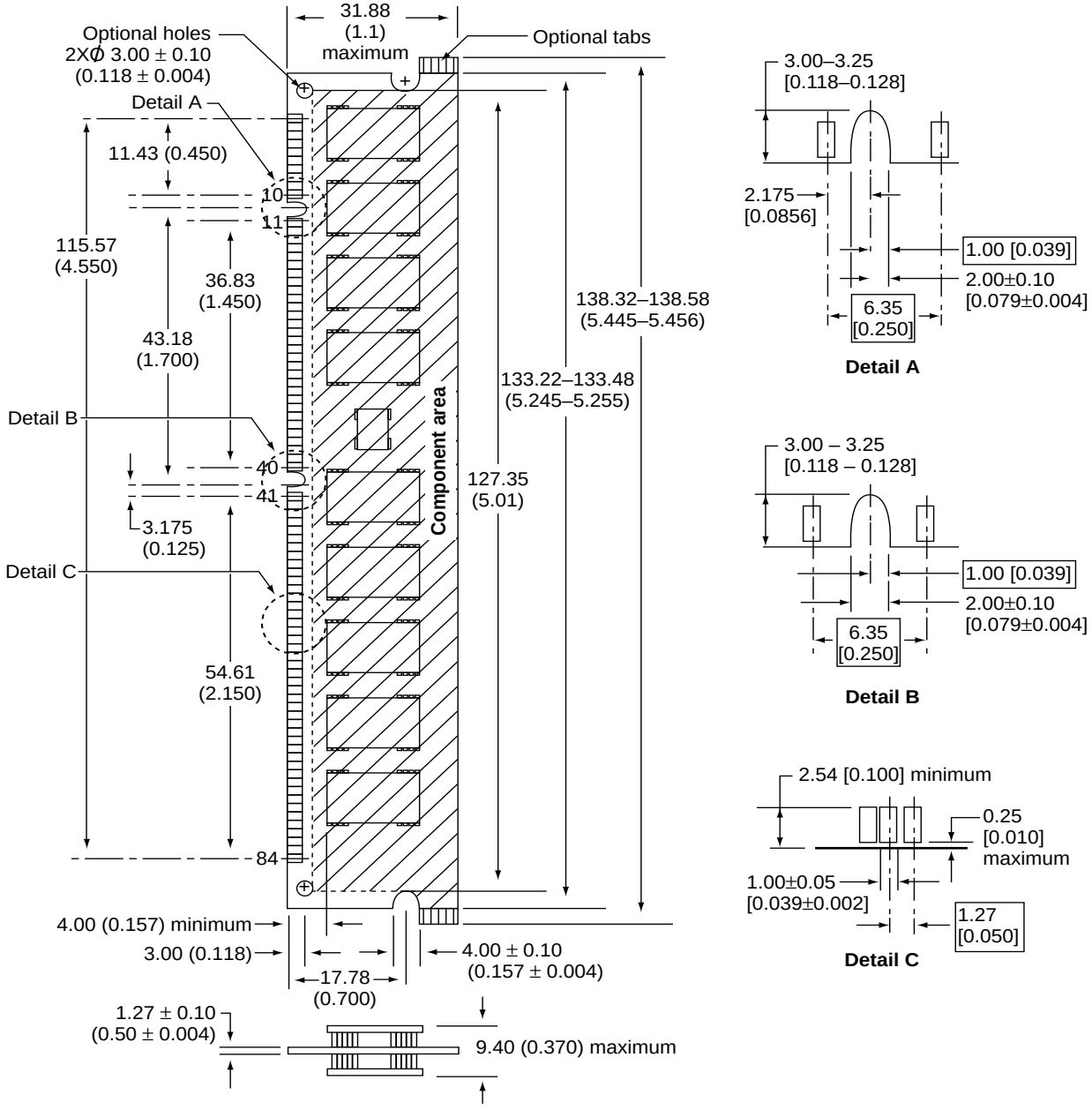
RAM DIMM Dimensions

Figure 4-1 shows the dimensions of the RAM DIMM.

IMPORTANT

The JEDEC MO-161 specification shows three possible heights for the DRAM DIMM. For Macintosh computers, developers should use only the shortest of the three: 1.100 inches. Taller DIMMs put excessive pressure on the DIMM sockets due to possible mechanical interference inside the case. ▲

Figure 4-1 Dimensions of the RAM DIMM



Note: dimensions are in millimeters (inches)

Second-Level Cache DIMM

The Power Macintosh 4400 logic board has a slot for a second-level (L2) cache on a DIMM.

The L2 cache DIMM contains the cache controller, tag, and data store memory. It is a lookaside cache, which is connected to the PowerPC processor bus.

Table 4-7 shows the pin and signal assignments on the L2 cache DIMM connector.

Table 4-7 Pin and signal assignments for the L2 cache DIMM connector

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	+5 V	41	A15	81	D63 (LSB)	121	A16
2	D31	42	A13	82	D62	122	A14
3	D30	43	+3.3 V	83	D61	123	A12
4	D29	44	A11	84	GND	124	A10
5	D28	45	A9	85	D60	125	A8
6	D27	46	A7	86	D59	126	GND
7	+5 V	47	A5	87	D58	127	A6
8	D26	48	A3	88	D57	128	A4
9	D25	49	+3.3 V	89	D56	129	A2
10	D24	50	A1	90	GND	130	A0 (MSB)
11	D23	51	/WT	91	D55	131	/DBB
12	D22	52	/GBL	92	D54	132	GND
13	+5 V	53	Reserved	93	D53	133	/CPU_BG
14	D21	54	/SRESET	94	D52	134	/CPU_BR
15	D20	55	+3.3 V	95	D51	135	L2_PRSNT
16	D19	56	TTYPE0	96	GND	136	Reserved
17	D18	57	TTYPE1	97	D50	137	TSIZ0
18	D17	58	TTYPE2	98	D49	138	GND
19	+5 V	59	TTYPE3	99	D48	139	TSIZ1
20	D16	60	TTYPE4	100	/CACHE_EN	140	TSIZ2
21	/L2_BR	61	+3.3 V	101	/TBST	141	/SHD
22	/L2_BG	62	D15	102	GND	142	D47

continued

Table 4-7 Pin and signal assignments for the L2 cache DIMM connector (continued)

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
23	TC0	63	D14	103	/CI	143	D46
24	TC1	64	D13	104	/RSRV	144	GND
25	+3.3 V	65	D12	105	Reserved	145	D45
26	/HRESET	66	D11	106	/CACHE_HIT	146	D44
27	/TEA	67	+5 V	107	/AACK	147	D43
28	/TS	68	D10	108	GND	148	D42
29	GND	69	D9	109	/TA	149	D41
30	SYS_CLK	70	D8	110	/ARTRY	150	GND
31	+3.3 V	71	D7	111	/ABB	151	D40
32	A31 (LSB)	72	D6	112	A30	152	D39
33	A29	73	+5 V	113	A28	153	D38
34	A27	74	D5	114	GND	154	D37
35	A25	75	D4	115	A26	155	D36
36	A23	76	D3	116	A24	156	GND
37	+3.3 V	77	D2	117	A22	157	D35
38	A21	78	D1	118	A20	158	D34
39	A19	79	+5 V	119	A18	159	D33
40	A17	80	D0 (MSB)	120	GND	160	D32

Table 4-8 defines the signals on the L2 cache DIMM connector.

Table 4-8 Signal descriptions for L2 cache DIMM connector

Signal name	Description
+5 V	Power supply voltage of +5 volts for tag RAM (5% tolerance)
+ 3.3 V	Power supply voltage of +3.3 volts for data RAM (5% tolerance)
GND	Ground
A(0-31)	Processor address bus signals 0 through 31
D(0-63)	Processor data bus signals 0 through 63; sampled on the rising edge of the CLK signal during a write cycle
/AACK	Address acknowledge, same as AACK_ signal on PowerPC 603e
/ARTRY	Address retry, same as ARTRY_ signal on PowerPC 603e

continued

Table 4-8 Signal descriptions for L2 cache DIMM connector (continued)

Signal name	Description
/ABB	Address bus busy, same as ABB_ signal on PowerPC 603e
/CI	Cache inhibit, same as CI_ signal on PowerPC 603e
/CPU_BG	Bus transaction granted, same as BG_ signal on PowerPC 603e
/CPU_BR	Bus transaction requested, same as BR_ signal on PowerPC 603e
/DBB	Data bus busy, same as DBB_ signal on PowerPC 603e
/GBL	Global transaction
/HRESET	Main logic board hardware reset
/L2_BG	Bus grant to L2 cache; used only in copyback mode
/L2_BR	Bus request from L2 cache; used only in copyback mode
CACHE_EN	Enables cache when high
L2_PRSNT	L2 cache present; tied directly to power rail on cache DIMM
/CACHE_HIT	Indicates L2 cache will source the data for the current cycle; inhibits main logic board memory controller
/RSRV	Reservation signal, same as RSRV_ signal on PowerPC 603e
Reserved	Do not use
/SHD	Shared, not used
/SRESET	Soft reset, same as SRESET_ signal on PowerPC 603e
SYS_CLK	System clock, same as SYSCLOCK signal on PowerPC 603e
/TA	Transfer acknowledge, same as TA_ signal on PowerPC 603e
/TBST	Transfer burst in progress, same as TBST_ signal on PowerPC 603e
TC(0-1)	Transfer code, same as TC signal on PowerPC 603e
/TEA	Transfer error acknowledge, same as TEA_ signal on PowerPC 603e
/TS	Transfer start signal, same as TS_ signal on PowerPC 603e
TSIZ (0-2)	Transfer size for the data transaction
TTYPE(0-4)	Transfer type, same as TT signal on PowerPC 603e
/WT	Write-through, same as WT_ signal on PowerPC 603e

Video RAM

The Power Macintosh 4400 logic board has a 120-pin video DIMM connector that allows the use of +5 V EDO DRAM, +3.3 V SDRAM, and +3.3 V SGRAM for video RAM

expansion. The video DIMM connector used on the Power Macintosh 4400 logic board is Burndy Corporation's part number ELF120GSC-3Z50 or equivalent. The connector is designed to support the pinout of the ATI 264VT-A4S2 graphics controller. The graphics controller recognizes the presence of pullup resistors on certain data bits on the DIMM to determine which type of memory is present. The video controller supports 1, 2, or 4 MB of RAM for video memory.

Note
No video performance advantage is gained with EDO video DIMMs larger than 2 MB. 4-MB video DIMMs built with SGRAM and SDRAM devices provide higher bandwidth performance. ◆

Table 4-9 shows the pin and signal assignments on the video DIMM connector.

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector

Pin	Signal name	Pin	Signal name
1	GND	61	GND
2	VA0	62	VA1
3	VA2	63	VA3
4	VA4	64	VA5
5	VA6	65	VA7
6	+5 V	66	+5 V
7	VA8	67	VA9
8	Reserved	68	Reserved
9	/VOE, (0) (SCLK)	69	/VOE(1)
10	/VWE(0)	70	/VWE(1)
11	GND	71	GND
12	/VRAS(0)	72	/VRAS(1)
13	/VCAS(0)	73	/VCAS(1)
14	/VCAS(2)	74	/VCAS(3)
15	/VCAS(4)	75	/VCAS(5)
16	+3.3 V	76	+3.3 V
17	/VCAS(6)	77	/VCAS(7)
18	VMD0	78	VMD1
19	VMD2	79	VMD3
20	VMD4	80	VMD5

continued

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector (continued)

Pin	Signal name	Pin	Signal name
21	GND	81	GND
22	VMD6	82	VMD7
23	VMD8	83	VMD9
24	VMD10	84	VMD11
25	VMD12	85	VMD13
26	+5 V	86	+5 V
27	VMD14	87	VMD15
28	VMD16	88	VMD17
29	VMD18	89	VMD19
30	VMD20	90	VMD21
31	GND	91	GND
32	VMD22	92	VMD23
33	VMD24	93	VMD25
34	VMD26	94	VMD27
35	VMD28	95	VMD29
36	+3.3 V	96	+3.3 V
37	VMD30	97	VMD31
38	VMD32	98	VMD33
39	VMD34	99	VMD35
40	VMD36	100	VMD37
41	GND	101	GND
42	VMD38	102	VMD39
43	VMD40	103	VMD41
44	VMD42	104	VMD43
45	VMD44	105	VMD45
46	+5 V	106	+5 V
47	VMD46	107	VMD47
48	VMD48	108	VMD49
49	VMD50	109	VMD51
50	VMD52	110	VMD53

continued

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector (continued)

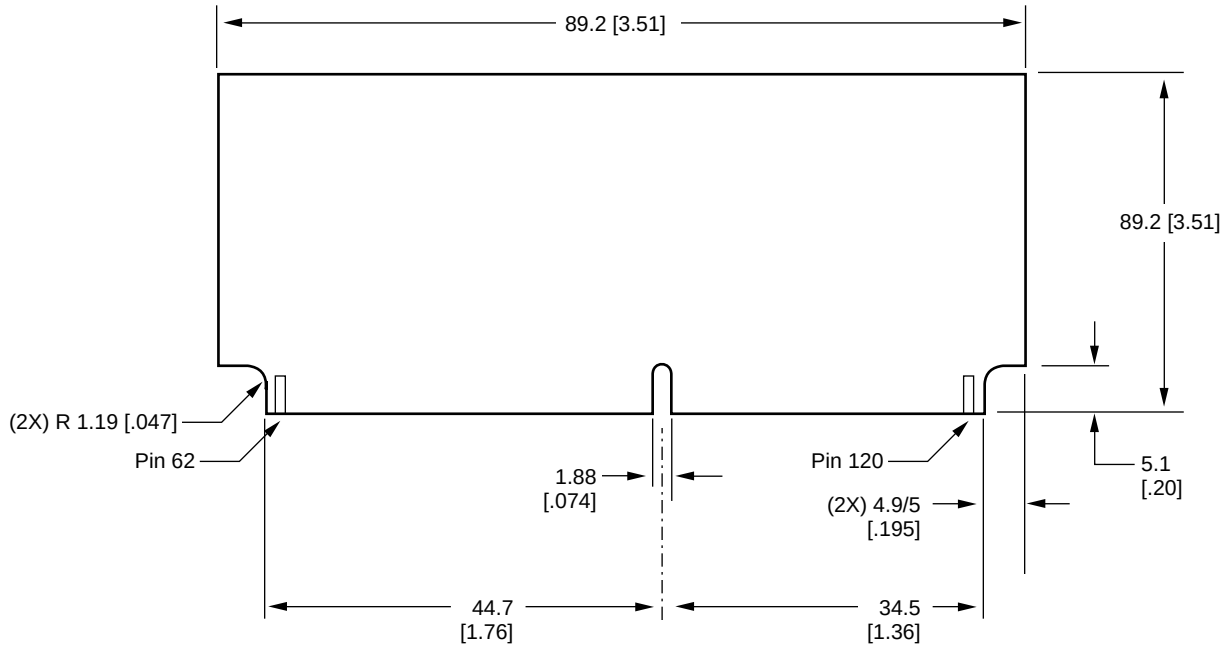
Pin	Signal name	Pin	Signal name
51	GND	111	GND
52	VMD54	112	VMD56
53	VMD56	113	VMD57
54	VMD58	114	VMD59
55	VMD60	115	VMD61
56	+3.3 V	116	+3.3 V
57	VMD62	117	VMD63
58	DSF	118	/CS0
59	Reserved	119	/CS1
60	TermPwr	120	TermGnd

The TermPwr signal on pin 60 is used only for clock termination of the SGRAM and SDRAM SCLK signal on pin 9.

Video RAM DIMM Card

Video DIMM cards for the Power Macintosh 4400 computer must be constructed as a four or more layer PCB substrate with one of the conductive layers on the PCB used for ground, not for signal routing. The dimensions for a 120-pin video DIMM card are shown in Figure 4-2.

Figure 4-2 Video DIMM card dimensions



PCI Expansion Slot

The Power Macintosh 4400 computer uses the industry-standard peripheral component interconnect (PCI) bus for an I/O expansion bus. The PCI bus is a 32-bit multiplexed address and data bus. The PCI expansion slot has a 33.33 MHz system clock.

PCI I/O expansion cards are mounted horizontally in a 90-degree straight-through adapter board, which is installed in the PCI expansion slot on the main logic board.

IMPORTANT

The Power Macintosh 4400 computer requires that PCI cards use the 5-volt signaling standard described in the *PCI Local Bus Specification*, Revision 2.0. ▲

The Power Macintosh 4400 computer accepts standard 6.88-inch and 12.283-inch PCI cards as defined by the *PCI Local Bus Specification*, Revision 2.0. The cards are required to use the standard ISA fence described in the specification.

The PCI expansion slots except two 6.88-inch PCI cards, or one 6.88-inch and one 12.283-inch PCI card. The middle slot on the PCI riser card is for 12.283-inch PCI cards. The 12.283-inch PCI cards do not fit in the top PCI expansion slot because of mechanical interference with the floppy drive housing.

The PCI expansion slots support all the required PCI signals and certain optional PCI signals. The supported PCI signals are listed in Table 4-4.

Table 4-10 PCI signals

Signal name	Description
AD [0–31]	Address and data, multiplexed
C/BE[0–3]	Bus command and byte-enable signals, multiplexed
PAR	Parity; used with AD and C/BE signals
FRAME#	Cycle frame; asserted to indicate a bus transaction
TRDY#	Target ready; selected device is able to complete the current phase
IRDY#	Initiator ready; master device is able to complete the current phase
STOP#	Stop; indicates the current target device is requesting the master to stop the current transaction
DEVSEL#	Device select; indicates that the driving device has decoded its address as the target of the current access
IDSEL	Initialization device select; used during configuration
REQ#	Request; indicates to the arbiter that the asserting agent requires access to the bus
GNT#	Grant; indicates to the agent that access to the bus has been granted
CLK	Clock; rising edge provides timing for all transactions
RST#	Reset; used to bring registers and signals to a known state
INTA#, INTB#, INTC#, INTD#	Interrupt request pins A, B, C, and D; wired together on each slot
LOCK#	Lock; indicates an operation that may require multiple transactions to complete
PERR#	Parity error; used to report data parity errors during PCI transactions excluding a Special Cycle transaction
SERR#	System error; used to report address parity errors, data parity errors during a Special Cycle, or any other system error that will be catastrophic

The PCI expansion slots on the Power Macintosh 4400 logic board do not support the optional 64-bit bus extension signals or cache support signals.

For more information about the PCI expansion slot, refer to *Designing PCI Cards and Drivers for Power Macintosh Computers.*

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