Developer Note

Xserve

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About This Note

This developer note describes Apple Computer's Xserve computer. The note provides information about the internal design of the computer, its input-output and expansion capabilities, and issues affecting compatibility.

This developer note is intended to help hardware and software developers design products that are compatible with the Macintosh products described here. If you are not already familiar with Macintosh computers or if you would simply like additional technical information, refer to Chapter A, "Supplemental Reference Documents."

The information is arranged in four chapters and two appendixes:

- Chapter 1, "Introduction" (page 11), gives a summary of the features of the Xserve computer, describes the physical appearance of the enclosure, and lists compatibility issues of interest to developers.

- Chapter 2, "Architecture" (page 23), describes the internal organization of the computer. It includes a functional block diagram and descriptions of the main components on the logic board.

- Chapter 3, "Input and Output Devices" (page 35), describes the built-in I/O devices and the external I/O ports.

- Chapter 4, "Expansion" (page 51), describes the expansion slots on the logic board and provides specifications for the expansion modules.

- Appendix A, "Supplemental Reference Documents" (page 55), provides sources of additional information about the technologies used in the Xserve computer.

- Appendix B, "Conventions and Abbreviations" (page 63), lists standard units of measure and other abbreviations used in this developer note.

About This Note

Introduction

The Xserve computer is the Macintosh server platform using the PowerPC G4 microprocessor. It has a rack-mount enclosure and includes server-oriented features such as ample internal storage, hot-pluggable drives, hardware monitoring, and tool-less access.

This developer note includes both the high-end slot load configuration and the basic cluster node configuration. The differences in the two Xserve configurations are identified throughout this document.

Hardware Features

Table 1-1 provides a list of the hardware features of the Xserve slot load and cluster node configuration computers. Each of the major features is described more fully later in this note, as indicated by the cross references.

Table 1-1   Hardware Features of the Slot Load and Cluster Node Xserve

Feature	Slot Load Xserve	Cluster Node Xserve
microprocessor speed	Dual or single PowerPC G4 microprocessor running at a clock frequency of 1.33 GHz. See "PowerPC G4 Microprocessor" (page 26).	Dual PowerPC G4 microprocessor running at a clock frequency of 1.33 GHz. See "PowerPC G4 Microprocessor" (page 26).
Memory caches	Internal 256 KB level 2 cache per processor and external 2 MB level 3 cache per processor. See "Cache Memory" (page 26).	
Processor system bus	64-bit wide data and 32-bit wide address, 167 MHz clock, supporting MaxBus protocol. See "Processor Bus" (page 27).	
RAM	Four DIMM slots for 184-pin DIMMs (dual inline memory modules) using DDR (double data rate) dynamic RAM devices. A minimum of 256 MB of RAM is installed in one of the slots. See "RAM Expansion" (page 51).	
ROM	ROM-in-RAM implementation with 1 MB of boot ROM. For information about the ROM, see "Boot ROM" (page 29). For information about the ROM-in-RAM implementation, see the references listed in "ROM-in-RAM Architecture" (page 57).	
Graphics card	PCI or AGP graphics card with a VGA connector for the monitor. See "Graphics Cards" (page 32).	No graphics card.

Table 1-1   Hardware Features of the Slot Load and Cluster Node Xserve

Feature	Slot Load Xserve	Cluster Node Xserve
Hard disk drive bays	Four drive bays for Ultra DMA/133 with independent buses and support for hot-pluggable drives using Apple Drive Modules. See "Hard Disk Drive Bays" (page 45).	One drive bay for Ultra DMA/133 with independent bus and support for hot-pluggable drive using Apple Drive Modules. See "Hard Disk Drive Bays" (page 45).
CD-ROM drive	Contains CD-ROM drive. See "CD-ROM Drive" (page 44).	Not available.
Combo drive	A CD-RW/DVD-ROM Combo drive is available as a build-to-order option. See "Combo (DVD-ROM/CD-RW) Drive (Optional)" (page 45).	Not available.
Hard disk	7200-rpm, hot-pluggable, 60 GB hard disk drive in one of the four drive bays. 180 GB build-to-order drive available.	7200-rpm, hot-pluggable, 60 GB hard disk drive.
USB ports	Two USB ports. See "USB Ports" (page 35).	
Ethernet	Two Ethernet ports for 10Base-T, 100Base-T, or 1000Base-T operation. One port is on the main logic board and one is on a network card in a slot. See "Ethernet Ports" (page 41).	One Ethernet ports for 10Base-T, 100Base-T, or 1000Base-T operation on the main logic board. See "Ethernet Ports" (page 41).
FireWire ports	Two FireWire 800 ports on back panel and one FireWire 400 on front. See "FireWire Ports" (page 37).	
PCI card expansion slots	Two expansion slots for PCI cards. See "PCI Expansion Slots" (page 53).	
PCI/AGP card slot	One half-length PCI or AGP slot for a graphics or networking card. See "PCI Expansion Slots" (page 53).	No AGP slot available.
Fan speed control	The system monitors the fan speeds and reports if speeds are outside acceptable range, indicating that a fan needs service.	

Features of the Enclosure

The Xserve computer has a rack optimized enclosure that is 1U (1.75") tall and 29 inches or less deep. The enclosure conforms to the industry standard for 19-inch rack mounting. For information about the standard, see the reference at "EIA Rack Standards" (page 60).

All the components in the computer are accessible without the use of tools.

Figure 1-1 shows the front panel of the slot load Xserve, which has a power button and light, an enclosure lock and light, a system identifier button and light, a FireWire 400 port, an Ethernet link LED, a slot-loading optical drive, and a two-by-eight LED matrix under software control.

Introduction

Figure 1-1   Xserve slot load front panel
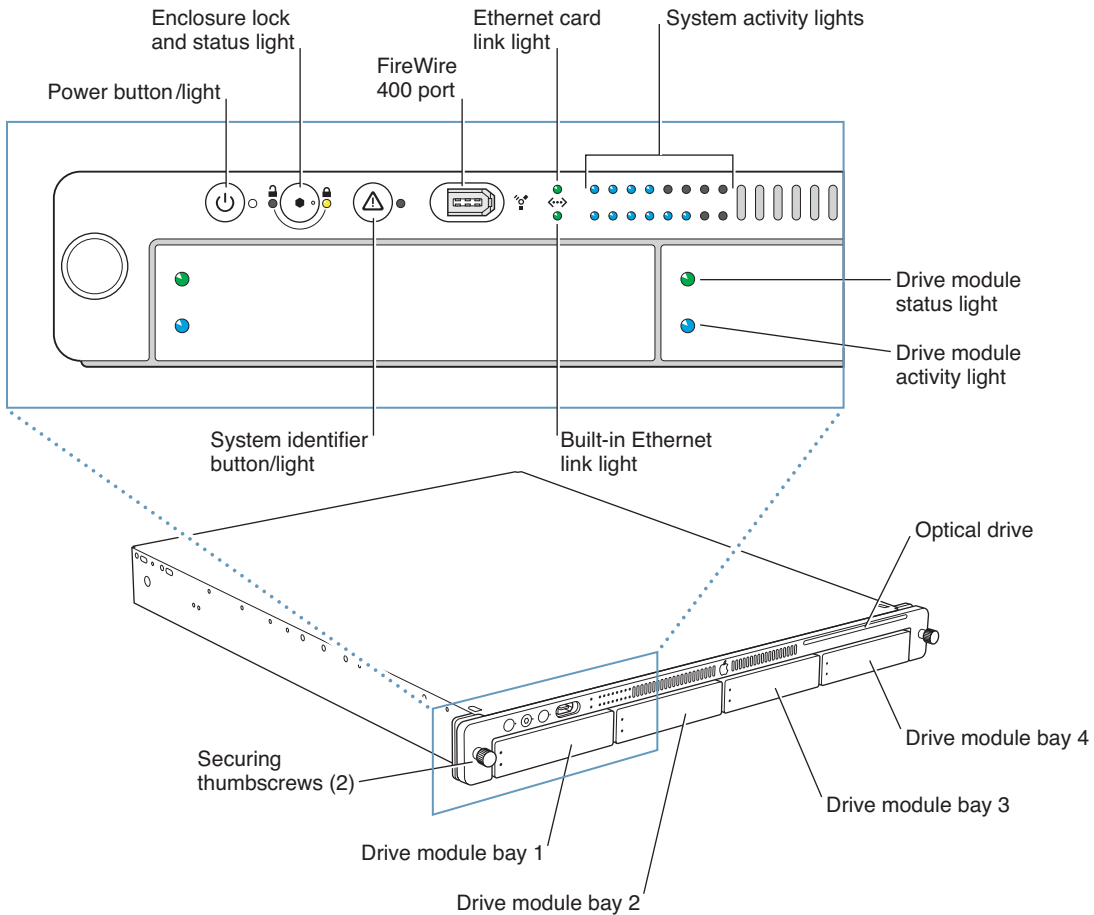
Figure 1-2 shows the back panel of the slot load Xserve, which has an A/C power socket, a gigabit Ethernet port, two FireWire 800 ports, a system identifier button and light, two USB ports, the serial console port, and the openings for ports on the PCI cards. PCI cards are secured to the enclosure by thumbscrews.

Figure 1-2   Xserve slot load back panel

Gigabit Ethernet port(s)   System identifier button/light

Power socket   PCI card expansion slots (3)

FireWire 800 ports (2)   VGA monitor port

USB ports (2)   Serial console port
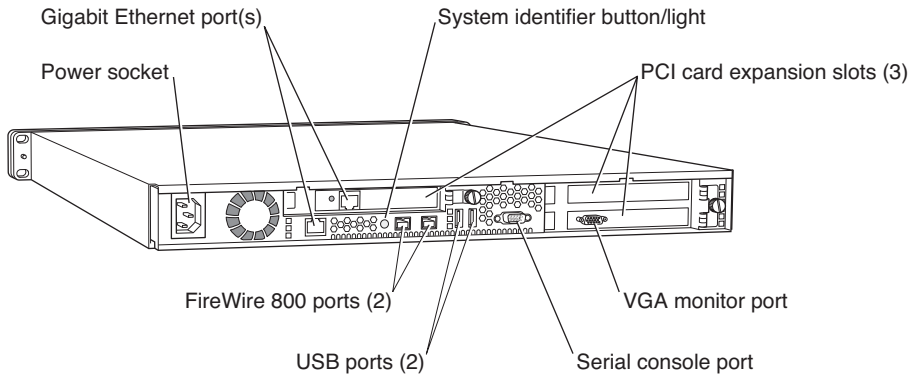
Figure 1-3 shows the front panel of the cluster node Xserve computer, which has a power button and light, an enclosure lock and light, a system identifier button and light, and a FireWire 400 port.

Figure 1-3   Xserve cluster node front panel

- System identifier button/light
- Enclosure lock and status light
- FireWire 400 port
- Power button/light
- System activity lights
- Securing thumbscrews (2)
- Built-in Ethernet link light
- Apple Drive Module bay
- Drive module status light
- Drive module activity light
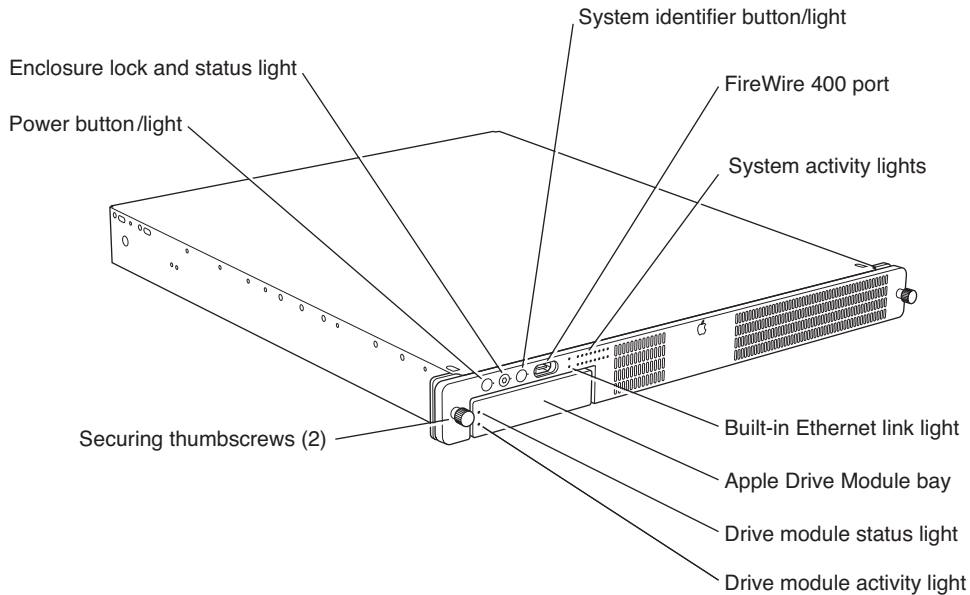
Figure 1-4 shows the back panel of the cluster node Xserve, which has an A/C power socket, two FireWire 800 ports, a system identifier button and light, two USB ports, the serial console port, and the openings for ports on the PCI cards. PCI cards are secured to the enclosure by thumbscrews.

Figure 1-4   Xserve cluster node back panel

Gigabit Ethernet port

System identifier button/light

Power socket

PCI card expansion slots (2)

FireWire 800 ports (2)

USB ports (2)

Serial console port
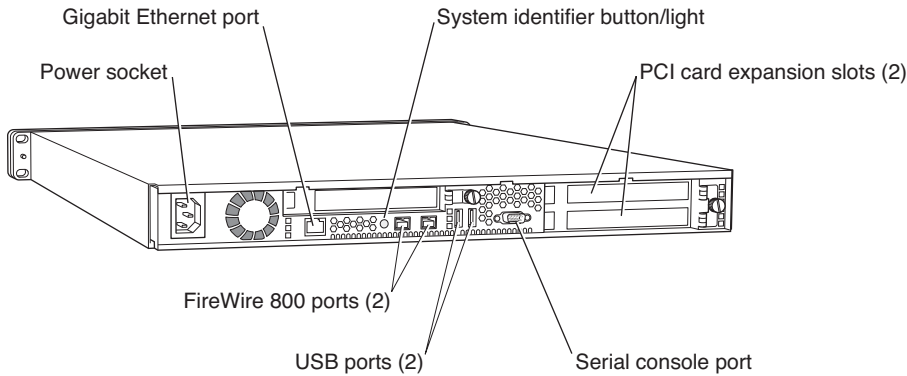
System Software

The Xserve slot load computer comes with Mac OS X Server installed. The Xserve cluster node computer comes with a restricted user license of Mac OS X Server installed.

Server Software Features

Here is a list of the key features of the system software on the Xserve computer. For more information, see the Xserve User's Guide.

- **UPS support:** A UPS vendor can provide a USB connection that connnects their device to the computer's UPS architecture and works with the Power Manager. The Server Monitor application can communicate with the UPS.

- **Auto restart after power failure:** Xserve hardware supports auto restart after power failure through software control. In the event of a power outage, an Xserve unit detects the return of power and performs an automatic restart.

- **Software administration tools:** The Terminal application in Mac OS X gives you access to a full array of command-line tools for software and system administration. The documentation ("man pages") for these tools is located in various subdirectories of the /usr directory.

- **Software updates:** The Software Update control panel supports headless selection and installation of updates.

- **SNMP:** Apple's SNMP stack on Xserve, implemented in Mac OS X Server, allows Xserve to be monitored by standard SNMP management consoles. In addition to the standard SNMP MIBs, Mac OS X Server provides MIBs for its core services. Xserve also provides hardware MIBs for key values. SNMP support is currently read-only.

Security Features

Here are the key security features supported by the system software on the Xserve computer.

- **Secure ports:** Xserve prevents mounting of CDs as well as hot-plugged USB and FireWire hard drives by means of an enclosure lock.

- **Secure remote management:** Xserve's remote monitoring and management tools run over encrypted links.

Storage Support

Here is a list of the key software features relating to hard disk storage on the Xserve computer.

- **Disk utilities tool:** You can use the filesystem consistency check and interactive repair tool, included with Mac OS X, to work on the Xserve computer's file system. For more information, launch the Terminal application in Mac OS X and enter the following line after the prompt:

```
man fsck
```

- **Remote volume configuration:** The system software can remotely configure newly mounted volumes.

- **USB and FireWire alerts:** Xserve's keyswitch security prevents unauthorized hot-plugging and mounting of a USB or FireWire hard drive.

Introduction

Management Support

Here are some of the management support features of the system software on the Xserve computer.

SNMP Implementation

The SNMP implementation in Mac OS X Server allows the Xserve computer to be monitored by standard SNMP management consoles.

The SNMP implementation on the Xserve is based on the net-snmp protocols. For more information, see the net-snmp page on the World Wide Web at

http://www.net-snmp.com/

Computer Feature Identification

Rather than reading the box flag or the model string and then making assumptions about the computer's features, applications that need to find out the features of the computer should use IORegistry calls to test for the features they require. IORegistry calls are part of the I/O Kit API. For more information, see the references listed at "I/O Kit" (page 57).

Asset management software that reports the kind of computer it is running on can obtain the value of the model property from the device tree root node. The entry banner of the Open Firmware user interface software displays the model property. Or, to display the model property from within the Open Firmware user interface, type the following to display the model property:

```
0 > dev /
0 > .properties
```

The "dev /" selects the root device and ".properties" displays all properties of the device selected.

For both slot load and cluster node Xserve computers, the value of the model property is RackMac1,2.

Introduction

Velocity Engine Acceleration

The Velocity Engine (an implementation of AltiVec) is the vector processing unit in the PowerPC G4 microprocessor. Some system software has been modified to take advantage of the accelerated processing that the Velocity Engine makes possible. System software has also been modified to support low-level operations using the Velocity Engine.

For complete information on the Velocity Engine, refer to the following Apple websites:

http://developer.apple.com/hardware/ve/

and

http://developer.apple.com/techpubs/macosx/CoreTechnologies/vDSP/vDSP.html

Introduction

Architecture

This chapter describes the architecture of the Xserve computer. It includes information about the major components on the logic boards: the microprocessor, the other main ICs, and the buses that connect them to each other and to the I/O interfaces.

Block Diagram and Buses

Figure 2-1 is a simplified block diagram of the Xserve computer. The diagram shows the main ICs and the buses that connect them together.

The architecture of Xserve is based on one or two PowerPC G4 microprocessors and two custom ICs: the U2 memory controller and bus bridge, and the KeyLargo I/O controller.

Architecture

Figure 2-1   Simplified block diagram
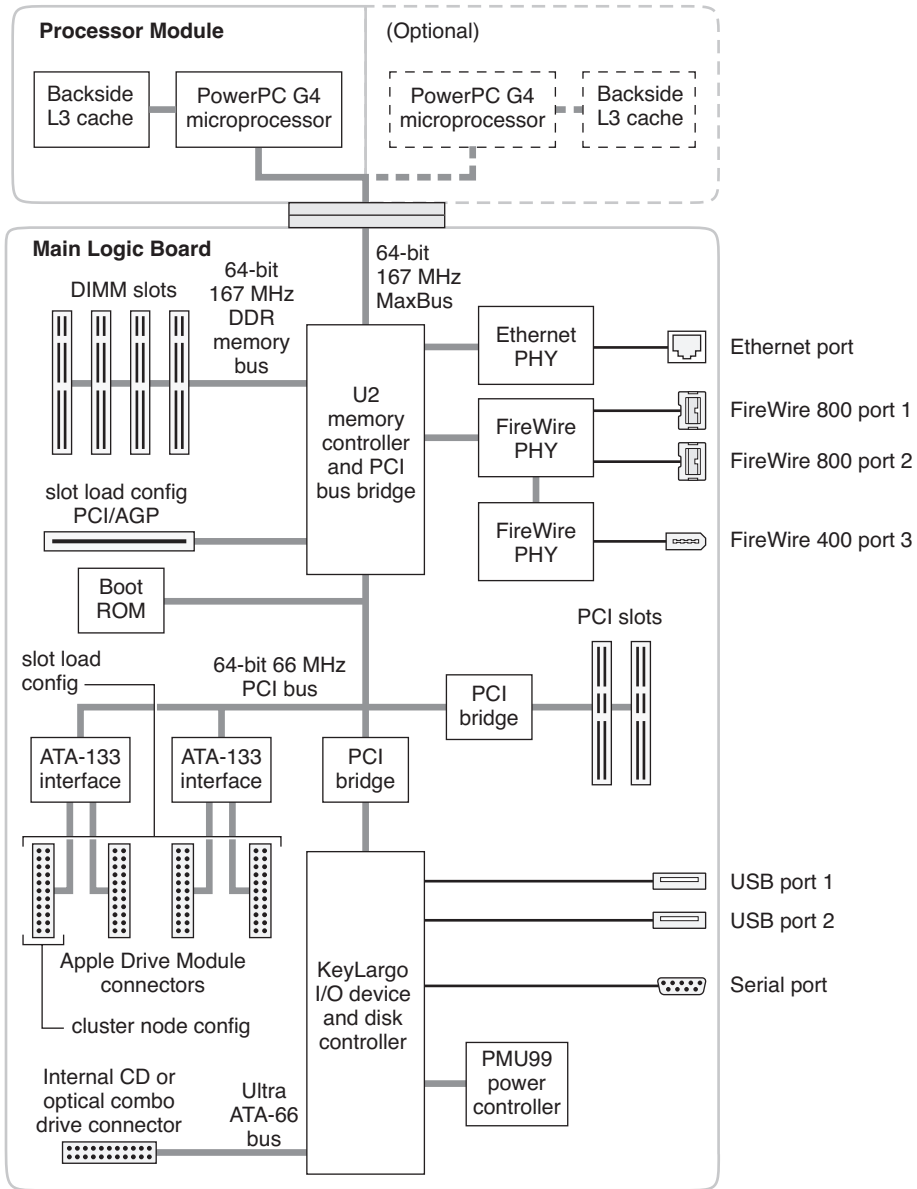
Architecture

Xserve has the following separate buses, not counting the processor's dedicated
interface to the backside cache.

- Processor bus: 167 MHz, 64-bit bus (known as the MaxBus) connecting a
  processor module with one or two microprocessors to the U2 IC

- Memory bus: 167 MHz double data rate (DDR), 64-bit bus connecting the main
  memory to the U2 IC.

- PCI buses: 66 MHz, 64-bit main PCI bus connecting the PCI card slots through
  a PCI-to-PCI bridge to the boot ROM, to the ATA-100 disk drive interfaces, and
  through another PCI-to-PCI bridge to the KeyLargo I/O controller.

- AGP/PCI combination bus: slot load configuration only — either 4X AGP bus
  for a graphics card or a 66 MHz (only) 32-bit PCI bus connected to the U2 IC

- Ultra ATA bus: ATA-capable bus connecting the internal CD drive to the
  KeyLargo I/O controller IC.

- Hard disk bus: ATA-133 connected independently to each drive.

The remainder of this chapter describes the architecture in three sections centered
around the processor module, the U2 memory controller and bridge IC, and the
KeyLargo I/O controller IC.

Processor Module

The processor module is a separate logic board that contains one or two G4
microprocessors and their external memory caches (if any).

The processor module is connected to the main logic board by way of a 300-pin
connector. To achieve the required level of performance, the signal lines that
connect the processor module and the main logic board are carefully matched in
length, loading, and impedance.

WARNING
DON'T TRY TO USE OLDER PROCESSOR CARDS! This
connector differs from those in earlier G4 computers and it is
not pin-compatible.

PowerPC G4 Microprocessor

The PowerPC G4 microprocessor used in the Xserve computer has many powerful features, including a pipelined system bus, called MaxBus, that is more efficient than the system bus on the PowerPC G3 microprocessors.

The PowerPC G4 used in the Xserve computer has the following features:

- 32-bit PowerPC implementation

- superscalar PowerPC core

- Velocity Engine (AltiVec technology): 128-bit-wide vector execution unit

- high bandwidth MaxBus

- fully symmetric multiprocessing capability

- dual 32 KB instruction and data caches (level one)

- built-in 256 KB backside L2 cache per processor

- support for up to 2 MB backside L3 cache per processor

- on-chip L3 tag storage

To find more information, see the reference at "PowerPC G4 Microprocessor" (page 55).

Cache Memory

In addition to the 256 KB L2 per processor cache built into the PowerPC G4 microprocessor, the processor card also has an external level 3 (L3) backside cache. The L3 cache consists of 2 MB of high-speed SRAM runing at a clock speed of 223 MHz (6:1 ratio).

Note: The Xserve computer does not use jumpers to control the clock speeds of the processor and cache.

Dual Processors

The dual-processor configuration of the Xserve computer has a processor card that contains two PowerPC G4 processors, each with its own external L3 cache. The dual-processor configuration allows applications that support multitasking to about double their performance.

Note: The cluster node Xserve computer is available only in dual configuration.

U2 Bridge and Memory Controller

The U2 custom IC is at the heart of the Xserve computer. It provides the bridging functionality between the processor, the memory system, the PCI-based I/O system, the AGP graphics slot, and the FireWire and Ethernet interfaces.

Processor Bus

The processor bus is a 167 MHz, 64-bit bus connecting the processor module to the U2 IC. In addition to the increased bus clock speed, the bus uses MaxBus protocols, supported by the U2 IC, for improved performance.

The MaxBus protocol includes enhancements that improve bus efficiency and throughput over the 60x bus. The enhancements include

- out of order completion
- address bus streaming
- intervention

Out of order completion allows the memory controller to optimize the data bus efficiency by transferring whichever data is ready, rather than having to pass data across the bus in the order the transactions were posted on the bus. This means that a fast DRAM read can pass a slow PCI read, potentially enabling the processor to do more before it has to wait on the PCI data.

Architecture

Address bus streaming allows a single master on the bus to issue multiple address transactions back-to-back. This means that a single master can post addresses at the rate of one every two clocks, as opposed to one every three clocks, as it is in the 60x bus protocol.

Intervention is a cache coherency optimization that improves performance for dual processor systems. If one processor modifies some data, that data first gets stored only in that processor's cache. If the other processor then wants that data, it needs to get the new modified values. In previous systems, the first processor must write the modified data to memory and then the second processor can read the correct values from memory. With intervention, the first processor sends the data directly to the second processor, reducing latency by a factor of ten or more.

Main Memory Bus

The main memory bus is a 167 MHz, 64-bit bus connecting the main memory to the U2 IC. Main memory is provided by up to four DDR333 SDRAM DIMMs. Supported DIMM sizes are 128, 256, and 512 MB. The memory slots will accept four 512-MB DIMMs for a maximum memory size of 2 GB. The minimum speed DDR is 2x167 MHz, which is DDR333 (PC2700).

For more information about memory DIMMs, see "RAM Expansion" (page 51).

Main PCI Bus

The main PCI bus connects the U2 IC to the boot ROM, through one PCI-to-PCI bridge the KeyLargo I/O controller, and through a second PCI-to-PCI bridge to the PCI slots. The PCI slots support "universal" PCI cards with 33 or 66 MHz operation. The PCI bus is a 66-MHz, 64-bit bus for the highest possible PCI card performance.

The PCI bus also supports the Apple Drive Module (ADM) interfaces: dual 2-channel ATA/133 controllers.

The U2 IC used in the Xserve computer supports a new PCI feature called Write Combining. This feature allows sequential write transactions involving the Memory Write or Memory Write and Invalidate commands to be combined into a single PCI transaction. The memory write transactions being combined must be to sequential, ascending, and non-overlapping PCI addresses. Placing an eieio or sync command between the write commands will prevent any write combining.

AGP / PCI Service

In the slot load Xserve computer, a combination slot supports either a PCI or an AGP card through a personality slot video card. When used for PCI, it supports 66 MHz 32-bit only operation. When used for AGP, it supports a 4X AGP bus. This slot does not provide any ADC power. For further details, see "PCI Expansion Slots" (page 53).

Boot ROM

The boot ROM consists of 1 MB of on-board flash EPROM. The boot ROM includes the hardware-specific code and tables needed to start up the computer. It uses Open Firmware to initialize the hardware, build the device tree, load an operating system, and provide common hardware access services.

Ethernet Controller

The U2 IC includes an Ethernet media access controller (MAC). As a separate I/O channel on the U2 IC, it can operate at its full capacity without degrading the performance of other peripheral devices. The U2 IC provides DMA support for the Ethernet interface.

The MAC implements the link layer. It is connected to a PHY interface IC that provides 10-BaseT, 100-BaseT, or 1000-BaseT operation over a standard twisted-pair interface. The operating speed of the link is automatically negotiated by the PHY and the bridge or router to which the Ethernet port is connected. For information about the port, see "Ethernet Ports" (page 41).

FireWire 400 and 800 Controllers

The U2 IC includes an IEEE 1394a FireWire 400 controller that implements the FireWire 400 link layer, supporting a maximum data rate of 400 Mbits per second. And, the U2 IC includes an IEEE 1394b FireWire 800 controller that implements the FireWire 800 link layer, supporting a maximum data rate of 800 Mbits per second.

Two physical layer (PHY) ICs connected to the U2 IC implement the electrical signaling protocol for the FireWire ports. The FireWire 400 port is located on the front panel; two FireWire 800 ports are located on the back panel.

While the PHYs are operating, they act as repeaters so that the FireWire bus remains connected. For more information, see "FireWire Ports" (page 37).

Note: The PHYs are powered as long as the computer is connected to AC power.

KeyLargo I/O Controller

The KeyLargo custom IC, the third major component of the Xserve architecture, is connected to the main PCI bus through a dedicated PCI-to-PCI bridge. It provides all the I/O functions except Ethernet and FireWire. The KeyLargo IC provides two USB root hubs, a UATA interface, and support for the LED display.

DMA Support

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the UATA interface and the LED matrix display. The DB DMA system provides a scatter-gather process based on memory-resident data structures that describe the data transfers. The DMA engine is enhanced to allow bursting of data files for improved performance.

Interrupt Support

The interrupt controller for the Xserve system is an MPIC cell in the KeyLargo IC. In addition to accepting all the KeyLargo internal interrupt sources, the MPIC controller accepts external interrupts from dedicated interrupt pins and serial interrupts from the U2 serial interrupt stream. The signals from the U2 IC are synchronized to the operation of the MPIC circuitry, so there is no additional interrupt latency on the U2 interrupts.

USB Interface

The KeyLargo IC implements two independent USB root hubs, each of which is connected to one of the ports on the back panel of the computer. The use of two independent hubs allows both USB ports to support high data rate devices at the

same time with no degradation of their performance. If a user connects a high-speed device to one port and another high-speed device to the other, both devices can operate at their full data rates.

The two external USB connectors support USB devices with data transfer rates of 1.5 Mbps or 12 Mbps. For more information, see "USB Ports" (page 35).

The USB ports comply with the Universal Serial Bus Specification 1.1 Final Draft Revision. The USB register set complies with the Open Host Controller Interface (OHCI) specification.

Serial Interface

The KeyLargo IC implements an RS-232-compatible serial port for use with a terminal. See see "Serial Port" (page 43). You can use the RI input on the serial port connector to wake the Xserve system from sleep mode.

Ultra ATA Interface

In the slot load Xserve, the KeyLargo IC provides an ultra ATA (UATA) interface. The UATA interface supports the CD-ROM drive or optional Combo drive mounted on the front panel.

For information about the optical drive, see "CD-ROM Drive" (page 44) or "Combo (DVD-ROM / CD-RW) Drive (Optional)" (page 45).

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the UATA interface.

Power Controller

The power management controller in Xserve is a microcontroller called the PMU99. It supports several modes of power management that provide significantly lower power consumption than previous systems.

System Monitor IC

The Xserve hardware contains an IC that monitors system voltages and the operation of both fans in the Xserve enclosure. Voltages monitored include 5 V main, 12 V main, 3.3 V trickle, 2.5 V sleep, logic Vcore and processor Vcore. The system monitor IC also contains a built-in temperature sensor that measures the hardware's ambient temperature to a resolution of 1 degree C; a second sensor on the processor card measures local processor temperature. Software can access the system monitor IC through the second U2 IIC bus at port address 0x5A.

System Activity Lights

Two rows of eight lights indicate system activity. In a server with a single processor, the rows of system activity lights operate together; in a dual-processor server, the rows of lights operate independently to show each processor's activity. In that case, CPU 0 is shown by the top row, CPU 1 by the bottom.

Device Identification

Each Xserve boot ROM contains a unique device serial number. However, because the boot ROM is a flash EPROM device, it is possible to overwrite the serial number and lose it irrecoverably. As an alternative, software that needs to identify an individual Xserve computer can access the `local-mac-address` property of its Ethernet node, which is set by Open Firmware at boot time. You can read this property using a tool such as IORegistry Explorer.

Graphics Cards

The Xserve slot load computer comes with a choice of graphics cards in the AGP/PCI slot; see "AGP/PCI Service" (page 29). The standard configuration has an ATI RV100 VGA/PCI graphics card with a VGA connector. The high-end configuration has an ATI R200 4x AGP card with DVI and ADC connectors, which can be driven simultaneously. The RV100 runs at 33 or 66 MHz; the R200 is clocked at 66 MHz.

Architecture

The Xserve slot load computer can boot headless (that is, without an attached monitor). While booted headlessly, the system actually creates a virtual display and draws into an off-screen buffer, without attempting to update a physical display. It is important that application design take this condition into account and not assume that graphics activity implies that a user is present.

The Xserve cluster node computer does not have a graphics card or internal graphics and is accessed via remote command line.

For more information about the features of the graphics cards and the monitors they support, see "VGA Connector" (page 46).

Architecture

Input and Output Devices

This chapter describes the Xserve computer's built-in I/O devices and the ports for connecting external I/O devices. Each of the following sections describes an I/O port or device.

USB Ports

The Xserve computer has two external Universal Serial Bus (USB) ports on the back. The USB ports can be used for connecting a keyboard and mouse as well as additional I/O devices such as printers, scanners, and low-speed storage devices.

Each USB port is connected to a separate USB root hub, allowing both USB ports to support 12 Mbps devices at the same time with no degradation of their performance.

For more information about USB on Macintosh computers, please refer to Apple Computer's Mac OS USB DDK API Reference and the other sources listed in "USB Interface" (page 59).

USB Connectors

The USB ports use USB Type A connectors, which have four pins each. Two of the pins are used for power and two for data. Figure 3-1 shows the connector and Table 3-1 shows the signals and pin assignments.

Input and Output Devices

Figure 3-1   USB connector
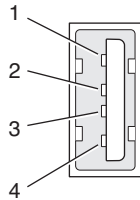
Table 3-1   Signals on the USB connector

Pin	Signal name	Description
1	VCC	+5 VDC
2	D–	Data –
3	D+	Data +
4	GND	Ground

The Xserve provides power for the USB ports at 5 V and up to 500 mA on each port. The ports share the same power supply; a short circuit on one will disable both ports until the short has been removed.

The USB ports support both low-speed and high-speed data transfers, at 1.5 Mbits per second and 12 Mbits per second, respectively. High-speed operation requires the use of shielded cables.

The Macintosh system software supports all four data transfer types defined in the USB specification.

FireWire Ports

The Xserve computer has three external FireWire ports: two FireWire 800 on the rear panel of the enclosure and one FireWire 400 on the front. The bilingual FireWire 800 ports have 9-pin connectors and support transfer rates up to 800 Mbps; the FireWire 400 port has a 6-pin connectors and supports transfer rates of 100, 200, and 400 Mbps. As long as security is not engaged, the Xserve computer can boot through FireWire; see "Booting from a FireWire Device" (page 41).

The FireWire ports

- provide a total of 15 watts of power when the computer system is on
- support up to 62 devices (each Xserve has 2 internal devices)
- provide bus repeating capability as long as the computer is connected to AC power

The FireWire hardware and software provided with the Xserve are capable of all asynchronous and isochronous transfers defined by IEEE standards 1394a and 1394b.

Developers of FireWire peripherals are required to provide device drivers. A driver for DV (digital video) is included in QuickTime 4.0 and later.

For more information about FireWire on Macintosh computers, please refer to the Apple FireWire website and the other sources listed in "FireWire Interface" (page 60).

FireWire 800 Connector

The FireWire 800 port on the Xserve computer is based on IEEE 1394b and enables a 800 Mbps transfer rate. FireWire 800 uses a 9-pin connector and is backwards compatible with original 1394 FireWire devices with 6-pin or 4-pin connectors. With

the appropriate cable, the 9-pin port works seamlessly with legacy FireWire devices. Cables are available to go from both 6-pin and 4-pin connectors to a 9-pin, and 9-pin to 9-pin.

Note: FireWire adapter cables are not included in the package.

The 9-pin FireWire 800 connector is shown in Figure 3-2. Its connector signals and pin assignments are shown in Table 3-2.

Figure 3-2   9-pin FireWire 800 connector
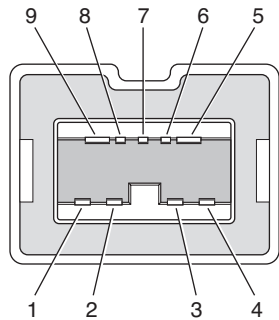
Table 3-2   Signals on the 9-pin FireWire 800 connector

Pin	Signal name	Description
1	TPB–	Twisted-pair B Minus
2	TPB+	Twisted-pair B Plus
3	TPA–	Twisted-pair A Minus
4	TPA+	Twisted-pair A Plus
5	TPA (R)	Twisted-pair A Ground Reference
6	VG	Power Ground

Table 3-2   Signals on the 9-pin FireWire 800 connector (continued)

Pin	Signal name	Description
7	SC	Status Contact (no connection; reserved)
8	VP	Power Voltage (18 to 25 V DC)
9	TPB (R)	Twisted-pair B Ground Reference

VP (pin 8) provides up to 15 W power, shared with the other FireWire connectors. The voltage on the power pin is 18 to 25 V.

The 9-pin FireWire port is capable of operating at 100, 200, 400, and 800 Mbps, depending on the device it is connected to. Using a cable with a 9-pin connector at one end and a 4-pin or 6-pin connector at the other, the 9-pin port is capable of directly connecting to all existing FireWire devices. Using a cable with 9-pin connectors at both ends, the 9-pin port is capable of operating at 800 Mbps.

The IEEE 1394b standard defines long-haul media using Cat 5 UTP and several kinds of optical fiber. The Xserve computer is interoperable with such cables but cannot be directly connected to them. To use long-haul cables, connect the computer to a 1394b hub that has the desired kind of long-haul connectors. If the hub has a bilingual port, that port can be connected to any of the computer's FireWire ports. If the hub has a beta-only port, it can be connected only to the computer's 9-pin port.

FireWire 400 Connector

The FireWire 400 port has a connector with six pins, as shown in Figure 3-3. The connector signals and pin assignments are shown in Table 3-3.

Figure 3-3   FireWire 400 connector
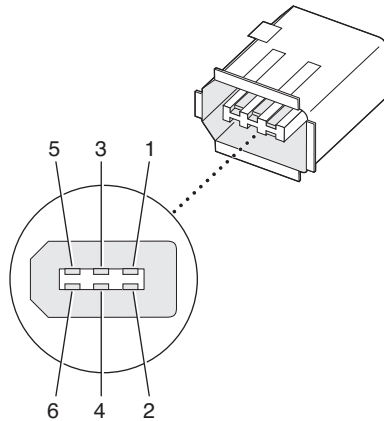
Table 3-3   Signals on the FireWire 400 connector

Pin	Signal name	Description
1	Power	Power (approximately 25 V DC)
2	Ground	Ground return for power and inner cable shield
3	TPB–	Twisted-pair B Minus
4	TPB+	Twisted-pair B Plus
5	TPA–	Twisted-pair A Minus
6	TPA+	Twisted-pair A Plus
Shell	—	Outer cable shield

The power pin provides up to 15 W total power for all three FireWire connectors. The voltage on the power pin can be from 18 to 25 V.

Pin 2 of the FireWire 400 connector is ground return for both power and the inner cable shield. In a FireWire cable with a 4-pin connector on the other end, the wire from pin 2 is connected to the shell of the 4-pin connector.

The signal pairs are crossed in the cable itself so that pins 5 and 6 at one end of the cable connect with pins 3 and 4 at the other end. When transmitting, pins 3 and 4 carry data and pins 5 and 6 carry clock; when receiving, the reverse is true.

Booting from a FireWire Device

Xserve can boot from a FireWire storage device that implements SBP-2 (Serial Bus Protocol) with the RBC (reduced block commands) command set. Detailed information is available from Developer Technical Support: dts@apple.com.

For additional information about the FireWire interface and the Apple APIs for FireWire device control, see the references shown in "FireWire Interface" (page 60).

Ethernet Ports

The cluster node Xserve provides an Ethernet port on the main logic board. Standard slot load Xserve configurations have two Ethernet ports: one on the main logic board and one on a network card. Both Ethernet ports support 10Base-T, 100Base-T, and 1000Base-T transfer rates. In operation, the actual speed of each link is auto-negotiated between the computer's PHY device and the hub, switch, or router to which it the port is connected. The Gigabit Ethernet card offers Jumbo Frame support. The Ethernet port on the main logic board does not offer Jumbo Frame support.

Note: When connecting an Xserve computer directly to another computer without using an Ethernet hub, a crossover cable is not required; circuits in the PHY detect the type of connection and switch the signal configuration as required.

The connectors for the Ethernet ports are RJ-45 connectors on the back of the computer. Table 3-4 shows the signals and pin assignments for 10Base-T and 100Base-T operation. Table 3-5 shows the signals and pin assignments for 1000Base-T operation.

Table 3-4   Signals for 10Base-T and 100Base-T operation

Pin	Signal name	Signal definition
1	TXP	Transmit (positive lead)
2	TXN	Transmit (negative lead)
3	RXP	Receive (positive lead)
4	–	Not used
5	–	Not used
6	RXN	Receive (negative lead)
7	–	Not used
8	–	Not used

Table 3-5   Signals for 1000Base-T operation

Pin	Signal name	Signal definition
1	TRD+(0)	Transmit and receive data 0 (positive lead)
2	TRD–(0)	Transmit and receive data 0 (negative lead)
3	TRD+(1)	Transmit and receive data 1 (positive lead)
4	TRD+(2)	Transmit and receive data 2 (positive lead)
5	TRD–(2)	Transmit and receive data 2 (negative lead)
6	TRD–(1)	Transmit and receive data 1 (negative lead)
7	TRD+(3)	Transmit and receive data 3 (positive lead)
8	TRD–(3)	Transmit and receive data 3 (negative lead)

To interconnect two computers for 1000Base-T operation, you must use 4-pair cable (Category 5 or 6).

The Ethernet interface in the Xserve conforms to the ISO/IEC 802.3 specification, where applicable, and complies with IEEE specifications 802.3i (10Base-T), 802.3u-1995 (100Base-T), and 802.3ab (1000Base-T).

Serial Port

The Xserve has an RS-232-compatible serial port for connecting a terminal, using a standard DB-9 plug. Figure 3-4 shows the mechanical arrangement of the pins on the serial port connector; Table 3-6 shows the signal assignments.

The serial ports includes a GPi (general-purpose input) signal on pin 7. The GPi signal connects to the data carrier detect input on the SCC (Serial Communications Controller). Alternatively, the GPi line can be connected to the receive/transmit clock (RTxCA) signal on the SCC. That connection supports devices that provide separate transmit and receive data clocks, such as synchronous modems.

Figure 3-4   Serial port connector

Table 3-6   Serial port signals

Pin	Signal name	Signal description
1	RLSD	Received line signal detector
2	RD	Received data
3	TD	Transmitted data

Table 3-6   Serial port signals

Pin	Signal name	Signal description
4	DRT	DTE ready
5	SGND	Signal ground
6	DCR	DCE ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator (wake up system)

Disk Drives

The slot load Xserve computer has four internal bays for hard disk drives and the cluster node Xserve computer has one internal bay. Depending on the configuration purchased, some bays may be empty. The slot load Xserve also contains a single CD-ROM drive or a build-to-order Combo drive.

CD-ROM Drive

The slot load Xserve computer has a slot-loading 24x-speed CD-ROM drive on the front of the enclosure.

The CD-ROM drive is connected by way of an Ultra DMA/66-capable interface on the KeyLargo IC. The interface supports DMA Mode 2 data transfers to and from the CD-ROM drive. The CD-ROM drive is an ATA-33 device and is Device 0 (master).

Combo (DVD-ROM/CD-RW) Drive (Optional)

The Xserve slot load computer can have an optional, slot-loading, build-to-order combination DVD-ROM and CD-RW drive.

The Combo drive can read DVD media and read and write CD media, as shown in Table 3-7. The DVD-ROM/CD-RW drive also provides DVD-Video playback. (The G4 microprocessor provides the MPEG 2 decoding.)

Table 3-7   Media read and written by the Combo drive

Media type	Reading speed	Writing speed
DVD-R	8x (CAV max)	–
DVD-ROM	8x (CAV max)	–
CD-R	24x (CAV max)	24x (ZCLV)
CD-RW	24x (ZCAV max)	10x (ZCLV, for high speed media)
CD or CD-ROM	24x (CAV max)	–

Digital audio signals from the Combo drive can be played through the sound outputs under the control of the Sound Manager.

Hard Disk Drive Bays

The slot load Xserve enclosure has four drive bays for fixed-media mass storage devices. For software applications, the bays are numbered one to four from left to right. In Open Firmware, the bays are numbered ultra0 to ultra3 from left to right. The cluster node Xserve enclosure has a single drive bay on the left, which is numbered as 1.

Each drive bay supports a hot-pluggable ATA/133 disk drive using an Apple Drive Module (ADM): a single unit that combines an ATA/133 hard drive mechanism, a translation board to support hot-plugability, and a drive carrier. A problematic drive can easily be removed and replaced with a new ADM while the system is running.

Figure 1-1 (page 15) shows a drive carrier with its two LEDs. The top one is a multicolor LED indicating drive state as follows:

■ Green: Drive in normal use by system

■ Yellow: Drive changing state (spinning up or down) or pre-failure warning

■ Red: Drive has failed

■ No color: No power to drive

The bottom (blue) LED indicates the individual drive's disk activity.

The monitoring software supports only drive modules manufactured by Apple.

The Xserve computer has four ATA/133 (ATA-6) buses, which also support ATA/100. Each bus is connected to a single ADM, which is permanently configured as a master. No jumpers are used and no drive configuration is needed.

VGA Connector

As a build-to-order option, the Xserve slot load computer can have a video graphics card installed. The card has a VGA connector for the video monitor.

The VGA connector is a three-row DB-15 (also called mini sub D15) connector for use with a VGA, SVGA, or XGA monitor. Figure 3-5 shows the pin configuration and Table 3-8 lists the signals and pin assignments.

Figure 3-5   VGA connector
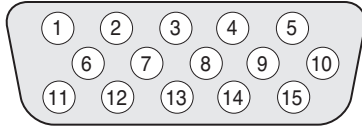
Table 3-8   Signals on the VGA connector

Pin	Signal name	Description
1	RED	Red video signal
2	GREEN	Green video signal
3	BLUE	Blue video signal
4	n.c.	No connect
5	GND	Ground
6	RED_RTN	Red video signal return
7	GREEN_RTN	Green video signal return
8	BLUE_RTN	Blue video signal return
9	n.c.	No connect
10	GND	Ground
11	n.c.	No connect
12	SDA	I2C data
13	HSYNC	Horizontal synchronization signal
14	VSYNC	Vertical synchronization signal
15	SCL	I2C clock

DVI-I Connector

If the graphics option is included in the slot load Xserve configuration, the external monitor connector is a DVI-I connector that carries both digital and analog video signals. Figure 3-6 shows the contact configuration. Table 3-9 and Table 3-10 list the signals and pin assignments.

Figure 3-6   DVI-I connector

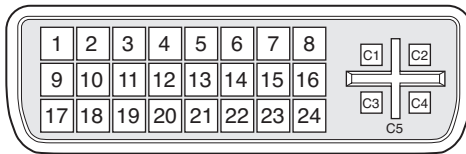**Table 3-9**   Main signals on the DVI-I connector

Pin	Signal name	Pin	Signal name
1	TMDS Data2–	13	TMDS Data3+
2	TMDS Data2+	14	+5V Power
3	TMDS Data2/4 Shield	15	Ground for +5V Power
4	TMDS Data4–	16	Hot Plug Detect
5	TMDS Data4+	17	TMDS Data0–
6	DDC Clock	18	TMDS Data0+
7	DDC Data	19	TMDS Data0/5 Shield
8	Analog Vertical Sync	20	TMDS Data5–
9	TMDS Data1–	21	TMDS Data5+

Table 3-9   Main signals on the DVI-I connector

Pin	Signal name	Pin	Signal name
10	TMDS Data1+	22	TMDS Clock Shield
11	TMDS Data1/3 Shield	23	TMDS Clock+
12	TMDS Data3–	24	TMDS Clock–

Table 3-10   MicroCross signals on the DVI-I connector

Pin	Signal name
C1	Analog Red Video
C2	Analog Green Video
C3	Analog Blue Video
C4	Analog Horizontal Sync
C5	Analog Common Ground Return

The graphics data sent to the digital monitor use transition minimized differential signaling (TMDS). TMDS uses an encoding algorithm to convert bytes of graphics data into characters that are transition-minimized to reduce EMI with copper cables, and DC-balanced for transmission over fiber optic cables. The TMDS algorithm also provides robust clock recovery for greater skew tolerance with longer cables or low-cost short cables. For additional information about TMDS, see the references shown in "Digital Visual Interface" (page 61).

Input and Output Devices

Expansion

This chapter describes the expansion features of the Xserve computer: the RAM expansion slots and the PCI expansion slots.

RAM Expansion

The main logic board has four RAM expansion slots for DDR SDRAM DIMMs. At least one of the RAM expansion slots contains a factory installed DIMM.

The DIMMs can be installed one or more at a time. The system supports linear memory organization; no performance gains are seen when two DIMMs of the same size are installed. Any supported size DIMM can be installed in any DIMM slot, and the combined memory of all of the DIMMs installed is configured as a contiguous array of memory.

The maximum memory size supported by the Xserve computer is 2 GB.

DIMM Specifications

The RAM expansion slots accept 184-pin DDR333 SDRAM DIMMs that are 2.5 volt, unbuffered, 8-byte, nonparity, and PC2700 compliant (2700 Mbytes/second bus bandwidth).

Mechanical Specifications

The mechanical design of the SDRAM DIMM is defined by the JEDEC Standard MO-206. To find this specification on the World Wide Web, refer to "RAM Expansion Modules" (page 58).

The maximum height of DIMMs for use in the Xserve computer is 1.25 inches.

Electrical Specifications

The electrical design of the SDRAM DIMM is defined by the JEDEC specification JESD21-C, MODULES4_20_4, Release 11b. To find this specification on the World Wide Web, refer to "RAM Expansion Modules" (page 58).

The Serial Presence Detect (SPD) EEPROM specified in the JEDEC standard is required and must be set to properly define the DIMM configuration. The EEPROM is powered on 3.3V. Details about the required values for each byte on the SPD EEPROM can be found on pages 68–70 of the JEDEC specification.

Important
For a DIMM to be recognized by the startup software, the Serial Presence Detect feature must be programmed properly to indicate the timing modes supported by the DIMM.

RAM Addressing

Signals A[0–12] on each SDRAM DIMM make up a 13-bit multiplexed address bus that can support several different sizes of SDRAM devices. Table 4-1 shows the address multiplexing modes used with various devices.

Table 4-1   Address multiplexing modes for SDRAM devices

Device size	Configuration	Row size	Column size
128 Mbits	4 M x 8 x 4	12	10
128 Mbits	2 M x 16 x 4	12	9
128 Mbits	1 M x 32 x 4	12	8

Table 4-1   Address multiplexing modes for SDRAM devices

Device size	Configuration	Row size	Column size
256 Mbits	8 M x 8 x 4	13	10
256 Mbits	4 M x 16 x 4	13	9
256 Mbits	2 M x 32 x 4	13	8

PCI Expansion Slots

The Xserve computer has dual expansion slots using the industry-standard peripheral component interconnect (PCI) bus. These slots support full-size PCI cards in either 64-bit/66-MHz or 32-bit/33-MHz configurations.

The PCI-only dual expansion slots accept 33-MHz or 66-MHz PCI cards with either 32-bit or 64-bit address and data buses. The PCI cards use power at +3.3 V. The slots accept standard 6.88-inch and 12.283-inch PCI cards as defined by the PCI Local Bus Specification, Revision 2.1. The cards are required to use the standard ISA fence described in the specification.

The slot load Xserve computer also has a combination AGP/PCI slot. The combination slot accepts half-size PCI 2.1 compatible 32-bit/66-MHz cards on a PCI riser card. The AGP/PCI riser card supports a 66 MHz-only 32-bit PCI 2.1 compatible card. The AGP/AGP riser card that is included if the AGP configuration is purchased supports a 4X AGP compatible card. These cards must follow the Universal Card Slot design. The AGP/PCI slot does not provide any ADC power.

The computer's case has openings in the back for access to I/O connectors on the PCI cards. The cards are secured in place by thumb screws accessible from the back of the computer.

The expansion slots support all the required PCI signals and certain optional PCI signals. The PCI slots support the optional 64-bit data bus extension signals.

Expansion

The maximum total power available for all PCI slots and the combination card slot is 50 watts. The card in the combination slot can account for up to 15 watts of that total.

Important
The user should first shut down the computer before removing or installing PCI expansion cards. Make sure the power light on the front is off. The Xserve computer does not support PCI hot-plugging functionality.

Supplemental Reference Documents

For more information about the technologies mentioned in this developer note, you may wish to consult some of the references listed in the following sections.

Apple Technical Notes

Apple Technical Notes answer many specific questions about the operation of Macintosh computers and the Mac OS. The technical notes are available on the Technical Note website at

http://developer.apple.com/technotes/

PowerPC G4 Microprocessor

Information about the PowerPC G4 microprocessor is available on the World Wide Web at

http://e-www.motorola.com/webapp/sps/site/
taxonomy.jsp?nodeId=01M98653

Velocity Engine (AltiVec)

Velocity Engine is Apple's name for the AltiVec vector processor in the PowerPC G4 microprocessor. Apple provides support for developers who are starting to use the Velocity Engine in their applications. Documentation, development tools, and sample code are now available on the World Wide Web, at

http://developer.apple.com/hardware/ve/index.html

and

http://developer.apple.com/techpubs/macosx/CoreTechnologies/vDSP/vDSP.html

AltiVec Technology Programming Environments Manual (AltiVec PEM) is a reference guide for programmers. It contains a description for each instruction and information to help in understanding how the instruction works. You can obtain a copy of the AltiVec PEM through the Motorola documentation site on the World Wide Web, at

http://e-www.motorola.com/webapp/sps/site/overview.jsp?nodeId=03M943030450467M0ymK5Nf2

Mac OS X

For access to Apple's developer documentation for Mac OS X, see the website at

http://developer.apple.com/techpubs/macosx/macosx.html

O'Reilly & Associates publishes a series of books about Mac OS X development. The books in this series have been technically reviewed by Apple engineers and are recommended by the Apple Developer Connection.

I/O Kit

The I/O Kit is part of Darwin, the operating system foundation for Mac OS X. The documentation for I/O Kit is available on Apple's Darwin website at

http://developer.apple.com/techpubs/macosx/Darwin/index.html

ROM-in-RAM Architecture

The system software in all current Macintosh computers uses a ROM-in-RAM approach, also called the New World architecture. For more information about this architecture, see Technical Note 1167, *NewWorld Architecture*, available on Apple's technical note website at

http://developer.apple.com/technotes/tn/tn1167.html

Open Firmware

The software architecture implemented on current Macintosh computers follows the standard defined by the Open Firmware IEEE 1274-1994 specification. Three Technical Notes provide an introduction to Open Firmware on the Macintosh platform. They are

TN 1061: *Open Firmware, Part I,* available on the technical note web site at

http://developer.apple.com/technotes/tn/tn1061.html

TN 1062: *Open Firmware, Part II*, at

http://developer.apple.com/technotes/tn/tn1062.html

TN 1044: *Open Firmware, Part III*, at

http://developer.apple.com/technotes/tn/tn1044.html

Other technical notes provide additional information about Open Firmware on the Macintosh.

TN 2000: *PCI Expansion ROMs and You*, at

http://developer.apple.com/technotes/tn/tn2000.html

TN 2001: *Running Files from a Hard Drive in Open Firmware*, at

http://developer.apple.com/technotes/tn/tn2001.html

TN 2004: *Debugging Open Firmware Using Telnet*, at

http://developer.apple.com/technotes/tn/tn2004.html

RAM Expansion Modules

The Xserve computer uses PC133 compliant, 184-pin DDR SDRAM DIMMs. The electrical characteristics of the DIMM are given in JEDEC specification JESD21-C, MODULES4_20_4, Release 11b. This specification can be found by using the search string "4_20_4" to search "By Document Number" in the JEDEC website at

http://www.jedec.org/DOWNLOAD/default.cfm

The mechanical characteristics of the DIMM package are given in JEDEC Standard MO-206. This specification can be found by using the search string "MO-206" to search "By Document Number" in the JEDEC website at

http://www.jedec.org/DOWNLOAD/default.cfm

Supplemental Reference Documents

ATA Devices

Information about ATA is available on the world wide web at

http://developer.apple.com/techpubs/macosx/Darwin/index.html

Information about the ATA standards is available at the Technical Committee T13 AT Attachment website, at

http://www.t13.org/

USB Interface

For more information about USB on the Macintosh computer, refer to Apple Computer's *Mac OS USB DDK API Reference*. Information is also available at

http://developer.apple.com/techpubs/hardware/DeviceManagers/usb/usb.html

USB game controllers are supported by the InputSprocket component of the Apple Games Sprockets software architecture. InputSprocket software and information about the InputSprocket APIs can be found at

http://developer.apple.com/games/

For full specifications of the Universal Serial Bus, you should refer to the USB Implementation Forum on the World Wide Web, at:

http://www.usb.org/developers/docs

FireWire Interface

For additional information about the FireWire 400 IEEE 1394a and FireWire 800 IEEE 1394b interfaces and the Apple APIs for FireWire software, refer to the resources available at

http://developer.apple.com/firewire

The IEEE 1394a nd 1394b standards are available from the IEEE; you can order that document electronically from the IEEE Standards Department website at

http://shop.ieee.org/store

You may also find useful information at the 1394 trade association's website at

http://www.1394ta.org/

EIA Rack Standards

To obtain a copy of the Electronics Industries Association standard for 19-inch racks and cabinets, visit the site "Availability of EIA Standards and Technical Publications" at the following URL.

http://www.eia.org/technology/availability.phtml

Serial Interface Standards

The Telecommunications Industry Association (TIA) is the trade organization that publishes the standards for the RS-232 serial interface. To obtain copies of the standards, you can contact the TIA's web page at

Supplemental Reference Documents

http://www.tiaonline.org/standards/

Digital Visual Interface

For information about transition minimized differential signaling (TMDS) used with digital video monitors, see the specification, Digital Visual Interface DVI Revision 1.0, available on the web site of the Digital Display Working Group (DDWG) at

http://www.ddwg.org/index.html

Supplemental Reference Documents

Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

Note: A note like this contains information that is of interest but is not essential for an understanding of the text.

Important
A note like this contains important information that you should read before proceeding.

Abbreviations

When unusual abbreviations appear in this developer note, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out.

Conventions and Abbreviations

Here are the standard units of measure used in developer notes:

A	amperes	mA	milliamperes
dB	decibels	μA	microamperes
GB	gigabytes	MB	megabytes
Hz	hertz	MHz	megahertz
in.	inches	mm	millimeters
k	1000	ms	milliseconds
K	1024	μs	microseconds
KB	kilobytes	ns	nanoseconds
kg	kilograms	sec.	seconds
kHz	kilohertz	V	volts
kΩ	kilohms	W	watts
lb.	pounds		

Other abbreviations used in developer notes include these:

ADM	Apple drive module
AGP	accelerated graphicsport
ATA	advanced technology attachment
ATAPI	advanced technology attachment, packet interface
CAS	column address strobe
CD-ROM	compact disc read-only memory
CLI	command line interface
DBDMA	descriptor-based direct memory access
DDR	double data rate, a type of SDRAM
DIMM	dual inline memory module
DMA	direct memory access
DRAM	dynamic random-access memory
EDO	extended data out DRAM device type
EIDE	extended IDE
EMI	electromagnetic interference

Conventions and Abbreviations

FTP	file transfer protocol
G4	Generation 4, the fourth generation of PowerPC microprocessors, incorporating AltiVec technology
GUI	graphic user interface
HID	human interface device, a class of USB devices
I2C	same as IIC
IIS	same as IIS
IC	integrated circuit
IDE	integrated device electronics
IEEE	Institute of Electrical and Electronics Engineers
IEEE 1274	the official specification for Open Firmware
IEEE 1394a	the official specification for FireWire 400
IEEE 1394b	the official specification for FireWire 800
IIC	inter-IC (an internal control bus)
IIS	inter-IC sound bus
I/O	input/output
ISO	International Organization for Standardization
JEDEC	Joint Electronics Devices Engineering Council
KVM	K Virtual Machine
L2	level 2 (refers to level of cache)
L3	level 3 (refers to level of cache)
LAN	local area network
MAC	media access controller
Mac OS	Macintosh Operating System
MIB	management infomation base
MOSSA	Mac OS Service Administrator
MPI	message passing interface
PCI	Peripheral Component Interconnect
PDC	primary domain controller
PHY	physical layer
PIO	polled input/output

Conventions and Abbreviations

RADIUS	Remote Authentication Dial-In User Service
RAID	redundant array of inexpensive drives
RAM	random-access memory
RAS	row address strobe
RBC	reduced block commands
RGB	a video signal format with separate red, green, and blue components
RISC	reduced instruction set computing
rms	root mean square
ROM	read-only memory
RS-232	standard serial interface
RS-422	standard serial interface
SBP	Serial Bus Protocol
SPD	Serial Presence Detect
SCSI	Small Computer System Interface
SCC	serial communications controller
SNMP	simple network management protocol
SDRAM	synchronous dynamic random access memory
SRAM	static random access memory
UPS	uninterruptible power supply
USB	Universal Serial Bus
TMDS	transition minimized differential signaling
VRAM	video RAM; used for display buffers

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